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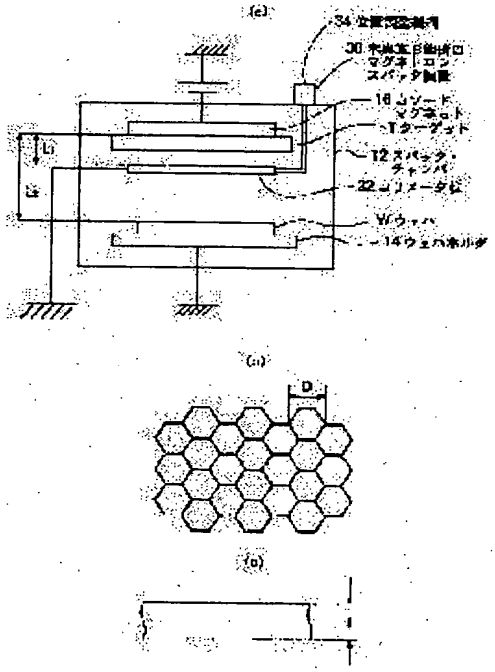
(54) MANUFACTURE OF SEMICONDUCTOR DEVICE AND SPUTTERING DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To sputter a high-melting point metal on the condition that the deterioration of the breakdown strength of a gate due to a sputtering device is not generated, in a method of manufacturing a semiconductor device, which is formed with a high-melting point metal silicide layer.

SOLUTION: A semiconductor device is manufactured into a structure, wherein a high-melting point metal is deposited on the whole surface of a silicon substrate formed with a gate electrode of a semiconductor element to form a high-melting point metal film and thereafter, when a heat treatment is performed on the surface of the substrate and a high-melting point metal silicide layer is formed on the interface between the surface of the substrate and the high-melting point metal film, the high-melting point metal film is sputtered and deposited by a magnetron sputtering unit on the condition that the amount Q of a charge to reach the gate electrode is less than 5 C/cm2. Moreover, a sputtering device 30 is constituted into a structure, wherein a collimater plate 32, which has a multitude of through holes penetrated from a target toward a wafer and consists of a conductor, is made to interpose between a target holder 16 and a wafer holder 14 in a state that the plate 32 is grounded.



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* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] The amount Q of charges which reaches said gate electrode in the manufacture approach of the semiconductor device which deposits a refractory metal all over the silicon substrate in which the gate electrode of a semiconductor device was formed, heat-treats after forming the refractory metal film, and forms a refractory metal silicide layer in an interface with said refractory metal film is 5 C/cm2. The manufacture approach of the semiconductor device characterized by to carry out sputter deposition of said refractory metal film with magnetron sputtering equipment on the conditions which become the following.
[Claim 2] Said magnetron sputtering equipment is the manufacture approach of the semiconductor device according to claim 1 characterized by being the configuration which sets up the magnitude of a target and carries out sputter deposition of said refractory metal film so that the plasma consistency maximum field may become the outside of said silicon substrate.
[Claim 3] Said magnetron sputtering equipment is the manufacture approach of the semiconductor device according to claim 1 characterized by being the configuration in which the holder magnet by the side of said silicon substrate carries out sputter deposition of said refractory metal for the wafer side face in which it has this silicon substrate, in the state of a wrap.
[Claim 4] Said magnetron sputtering equipment is the manufacture approach of the semiconductor device according to claim 1 characterized by being the configuration which sets up the reinforcement of the holder magnet by the side of this wafer, and carries out sputter deposition of said refractory metal so that the field of plasma consistency max may become the upper part from the wafer which has said silicon substrate.
[Claim 5] Said magnetron sputtering equipment is the manufacture approach of the semiconductor device according to claim 1 characterized by being the configuration which carries out sputter deposition of said refractory metal where the collimation plate of a conductor is inserted in the space between a target and the wafer which has said silicon substrate.
[Claim 6] Said collimation plate is the manufacture approach of the semiconductor device according to claim 5 characterized by a configuration on top being reticulated.
[Claim 7] Said refractory metal is [claim 1 characterized by being any 1 metal of titanium, cobalt, and nickel thru/or] the manufacture approach of a semiconductor device given in any 1 term among 6.
[Claim 8] The sputtering system characterized by to make it intervene where the collimation plate which consists of a conductor which has many through tubes penetrated towards the wafer between the target holder and the wafer holder from the target in the sputtering system which is equipped with the wafer holder holding the wafer on which a target metal is made to deposit as is made to meet the target held at the target holder and a target, and carries out sputtering of the target metal on a wafer is grounded.
[Claim 9] A collimation plate is the 1st spacing D1 to a target electrode holder. It is the 2nd spacing D2 below. Sputtering system according to claim 8 characterized by being arranged at intervals of the above range.
[Claim 10] The 1st spacing D1 It is 50mm and is the 2nd spacing D2. Sputtering system

according to claim 10 characterized by being 24mm.
[Claim 11] The sputtering system according to claim 9 or 10 characterized by having positioned the collimation plate in spacing of said range, and having a justification means to hold.
[Claim 12] A collimation plate is a sputtering system given in any 1 term of the claims 8–11 characterized by the aspect ratio of a through tube being 1.3 or less reticular lamina or more in 0.7.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the manufacture approach of an MOS mold field-effect transistor (MOSFET) of attaining low resistance-ization, by starting the manufacture approach of a semiconductor device, especially silicide-izing the gate, the source, and a drain front face in self align. Moreover, in case this invention forms the refractory metal silicide film in a gate electrode, as degradation of the withstand voltage of gate oxide does not arise, it relates to the sputtering system which can carry out the spatter of the refractory metal on the polish recon film.
[0002]
[Description of the Prior Art] There is an approach indicated by JP,2-45923,A in the conventional salicide process known as one of the manufacture approaches of a semiconductor device. The manufacture approach of this conventional semiconductor device is explained with reference to drawing of longitudinal section shown in order of the process of drawing 3 (a) - drawing 3 (d).
[0003] As shown in drawing 3 (a), the N well 302 is formed in the P type silicon substrate 301 by the known approach. Subsequently, field oxide 303 is formed in the front face of the P type silicon substrate 301 by the selective oxidation method as a field insulator layer. To the active region surrounded by this field oxide 303, gate dielectric film 304 and polycrystalline silicon, such as silicon oxide, are grown up one by one, Lynn is doped by known technique to polycrystalline silicon, and reduction of the electric resistance of polycrystalline silicon is aimed at. Subsequently, by the photolithography method and the dry etching method which are known technique, pattern NINGU of the polycrystalline silicon is carried out, and the gate electrode 305 is formed.
[0004] Next, with the photolithography method and ion-implantation, as shown in drawing 3 (a), the low-concentration N type impurity diffused layer 313 and the low-concentration P type impurity diffused layer 314 are formed. Subsequently, the sidewall 306 which consists of silicon oxide or a silicon nitride is formed in the side face of the gate electrode 305 using a known chemical-vapor-deposition (CVD) technique and a known etching technique.
[0005] Next, as shown in drawing 3 (b), the N type impurity diffused layer 307 and the P type impurity diffused layer 308 are formed with the photolithography method and ion-implantation. In this way, the N type source drain field 307 and the P type source drain field 308 are formed as LDD structure. Subsequently, the natural oxidation film of the front face of polycrystalline silicon and a semi-conductor substrate front face which is a gate electrode is removed, for example, sputter deposition of the titanium film 309 is carried out.
[0006] Next, as shown in drawing 3 (c), only the titanium film 309 which contacts silicon in nitrogen-gas-atmosphere mind 700 degrees C or less by carrying out rapid heat treatment (following, RTA) is silicide-ized, and the titanium silicide layer 310 of C49 mold structure is formed. Moreover, in this case, some of titanium film 309 in contact with field oxide 303 and a sidewall 306 and titanium film on a semi-conductor substrate are nitrided, and it serves as the titanium nitride film 311.

[0007] Next, as shown in drawing 3 (d), by mixed liquor, such as aqueous ammonia and hydrogen peroxide solution, etc., wet etching is carried out alternatively and only unreacted titanium and the titanium nitride film 311 are removed. Subsequently, hot (800 degrees C or more) RTA is performed rather than the above-mentioned RTA, and the titanium silicide layer 312 of C54 mold structure where electrical resistivity is lower than the titanium silicide layer 310 of the aforementioned C49 mold structure is formed.
[0008] By using the salicide process shown above, since the surface parts of polycrystalline silicon 305, N type, and the P type impurity diffused layers 307 and 308 are silicide-ized in self align, low resistance is formed, and improvement in the speed of a device can be attained. This salicide process has the advantage which can carry out [silicide]-izing alternatively only within the field to need.
[0009] By the way, generally, conventional magnetron sputtering equipment 10 equips with the cathode magnet 16 holding Target T the wafer holder 14 which makes Wafer W lay in the spatter chamber 12, and the location which estranges to Wafer W and meets it, as shown in drawing 8 . It had become a problem, when the chip which poor insulation produced in gate oxide was generated in generating on a wafer, especially a wafer periphery in many cases and the product yield was raised, in case the spatter of the Co was carried out and Co silicide electrode was formed on a polish recon gate electrode, using conventional magnetron sputtering equipment 10.
[0010] Here, using conventional magnetron sputtering equipment 10, the spatter of the Co is carried out on the polish recon of a gate electrode on the following spatter conditions, Co film is formed, and the result of having given RTA subsequently and having examined the quality of the withstand voltage of gate oxide for Co silicide-ization for every chip of a wafer after **** is shown. In an exam, using conventional magnetron sputtering equipment 10, as shown in drawing 9 , the spatter of the Co is carried out on the polish recon film 22 of the gate electrode formed on the silicon substrate 20, the Co film 24 is formed, subsequently RTA is given, and Co silicide layer is formed. Drawing 9 shows the condition of having formed the Co film 24 on the polish recon film 22 of a gate electrode by sputtering. The sidewall which 26 become from SiN etc., and 28 are gate oxide among drawing 9 .
Sputtering condition chamber pressure : 5 - 15mTorr quantity of gas flow Ar/50 - 100 scc/m spatter power : : In 1.5kW, however Co sputtering using conventional magnetron sputtering equipment 10 As shown in drawing 11 , especially to the gate oxide of the chip of the periphery of a wafer As poor insulation occurred and the withstand voltage of gate oxide showed the percentage to the chip of the whole wafer of the good chip beyond a predetermined value, and the so-called rate of an excellent article to drawing 19 together with the result of the example 1 of an experiment, and the example 2 of an experiment, it was about 46%. At drawing 11 , it is painted for the chip which poor insulation black [the chip which serious poor insulation has generated in gate oxide], and slight has generated in gray.
[0011]
[Problem(s) to be Solved by the Invention] However, by the manufacture approach of the above-mentioned conventional semiconductor device, after forming gate polish recon, when sputter deposition of the refractory metal was carried out on gate polish recon, on that occasion, the gate electrode 305 carried out the charge up with the charge generated from the plasma, and there was a problem that gate pressure-proofing deteriorated.
[0012] Although a salicide process is an effective approach as an approach of forming silicide only on a gate electrode and a diffusion layer, the natural oxidation film of the front face of the gate electrode 305 is removed for the substrate structure at the time of carrying out the spatter of the refractory metal, and, as for the gate electrode 305, an impurity is already doped, and it has become the floating gate.
[0013] Therefore, at the time of a spatter, a charge is generated in the gate polar zone at the moment of the shutter having opened from the discharge at the time during spatter discharge of standby, and sputter deposition being started especially, to a wafer, the charge flows gate dielectric film 304, and the problem that gate pressure-proofing deteriorates occurs. this phenomenon -- the thickness of gate dielectric film 304 -- thin-film-izing -- it is integrated highly -- it has been a serious problem as it is alike and it takes, and it is remarkable and

detailed-ization progresses.
[0014] This invention was made in view of the above-mentioned point, and aims at offering the manufacture approach of the semiconductor device which carries out the spatter of the refractory metal on the conditions which degradation of the gate pressure-proofing by the sputtering system does not produce in the manufacture approach of the semiconductor device which forms a refractory metal silicide layer between the insulator layers alternatively formed on a semi-conductor substrate.
[0015] Moreover, other purposes of this invention are to offer the manufacture approach of a semiconductor device that high-reliability and the MOS mold field-effect transistor in which the reduction in resistance is possible can be manufactured.
[0016] Moreover, as mentioned above, when carrying out the spatter of the refractory metals, such as Co, Ti, nickel, and W, on the polish recon film and performing silicide-ization using conventional magnetron sputtering equipment, there was a problem that the insulation of gate oxide fell. Then, in case the further purpose of this invention forms the refractory metal silicide film in a gate electrode, it is offering the sputtering system which can carry out the spatter of the refractory metal on the polish recon film as degradation of the withstand voltage of gate oxide does not arise.
[0017]
[Means for Solving the Problem] For this invention, the amount Q of charges which reaches a gate electrode in the manufacture approach of the semiconductor device which deposits a refractory metal all over the silicon substrate in which the gate electrode of a semiconductor device was formed in order to attain the above-mentioned purpose, heat-treats after forming the refractory metal film, and forms a refractory metal silicide layer in an interface with the refractory metal film is 5 C/cm2. It is the conditions which become the following and is made to carry out sputter deposition of the refractory metal film with magnetron sputtering equipment.
[0018] Here, above magnetron sputtering equipment is a configuration which sets up the magnitude of a target and carries out sputter deposition of the refractory metal so that the plasma consistency maximum field may become the outside of a silicon substrate.
[0019] Moreover, the configuration in which the holder magnet by the side of a silicon substrate carries out sputter deposition of the refractory metal for the wafer side face in which it has a silicon substrate, in the state of a wrap is sufficient as the above-mentioned magnetron sputtering equipment, and the configuration which sets up the reinforcement of the holder magnet by the side of a wafer, and carries out sputter deposition of the refractory metal is sufficient as it so that the field of plasma consistency max may become the upper part from the wafer which has a silicon substrate.
[0020] Furthermore, the configuration which carries out sputter deposition of the refractory metal where the collimation plate of a conductor is inserted in the space between a target and the wafer which has a silicon substrate is sufficient as above magnet RONSUPATTA equipment. In addition, as for the above-mentioned refractory metal, it is desirable that it is any 1 metal of titanium, cobalt, and nickel.
[0021] The amount Q of charges which reaches a gate electrode in this invention is 5 C/cm2. Sputter deposition of a refractory metal is performed on the conditions which become below, and it is made not to produce degradation of gate pressure-proofing.
[0022] An operation of this is explained. After drawing 4 etches the natural oxidation film using fluoric acid, it carries out sputter deposition of the titanium, and, subsequently shows the rate of an excellent article of gate pressure-proofing of the wafer which carried out wet etching of the deposited titanium by the mixed liquor of aqueous ammonia and hydrogen peroxide solution, without heat-treating. What was measured as a comparison, without performing a spatter is shown.
[0023] Since the poor initial proof pressure of the gate has happened and gate pressure-proofing deteriorates sharply during a spatter when the spatter of the titanium is carried out and it carries out wet etching immediately, the rate of a gate excellent article in that case has a low rate of an excellent article compared with the rate II of a gate excellent article when not carrying out the spatter of the titanium to drawing 4 , as I shows.

[0024] In case sputter deposition of drawing 5 is carried out, it shows the rate of a gate proof-pressure excellent article at the time of carrying out sputter deposition of the rate of a gate proof-pressure excellent article at the time of inserting a collimation plate between a wafer and a target without inserting a collimation plate, and the rate of a gate proof-pressure excellent article when not carrying out sputter deposition by comparison. Without performing a spatter postheat treatment like drawing 4 also in this case, wet etching was carried out and it has measured.

[0025] It turns out that it is 100% like the rate V of a gate proof-pressure excellent article when not carrying out sputter deposition, and degradation of the gate pressure-proofing by the spatter does not take place compared with the rate of a gate proof-pressure excellent article as III shows, when the spatter of the titanium is carried out and it carries out wet etching to this drawing immediately, but good gate pressure-proofing is obtained as IV shows the rate of a gate proof-pressure excellent article at the time of inserting a collimation plate between a wafer and a target when carrying out sputter deposition to drawing 5 .

[0026] In this case, the amount Q of charges which the charge which should reach a wafer flows to a collimation plate since the collimation plate is inserted between the wafer and the target, the charge up of a gate electrode is controlled, and reaches a gate electrode is 5 C/cm2. It is because sputter deposition which becomes below is made.

[0027] Usually, a collimation spatter is for depositing titanium on the pars basilaris ossis occipitalis of a contact hole with a sufficient anisotropy, and improving the coverage of the spatter film. However, it is not necessary to carry out using an established collimation plate, and the result obtained using the collimation spatter and the same result are obtained in this case that the reticulated plate grounded electrically should just be inserted between the wafer and the target, for example.

[0028] Thus, when carrying out sputter deposition of the refractory metal on a floating-gate electrode with the Salicide structure, it is possible from the plasma whether make the generated charge whether make it not generate an unnecessary charge or not reach a wafer as an approach of controlling the amount of charges which reaches to a wafer. Therefore, a gate proof-pressure property can be raised by combining above-mentioned two kinds or them.

[0029] In order that this invention person might realize the sputtering system which can attain the purpose of this invention mentioned above, the cause which the poor insulation of gate oxide generates arrived at the wafer front face, and the charged particle near the target found it out after research, when it was in penetrating the polish recon film and gate oxide of a gate electrode, and intruding a silicon substrate. That is, it was surmised that the cause which degradation of the withstand voltage of gate oxide produces was because the probability of collision which a charged particle comes flying from the high charged-particle consistency field which exists near the plasma (wafer side), and collides with a wafer increases. The field where a plasma consistency is high is concentrated on the periphery rather than the center section about the diameter direction of a target so that clearly from the Heroux Gen measurement of a target. And although the field where a plasma consistency is high is seen in the direction which faces to a wafer from a target and it exists near the **** of a target, it is thought that the field where a charged-particle consistency is high exists in the wafer side of a plasma field rather. Then, in order that a charged particle may prevent coming flying on a wafer and colliding, it is a location near a target, the collimation plate has been arranged in the location moreover slightly separated from the plasma field to the wafer side, and it hit on an idea of catching a charged particle with a collimation plate, and further, the physical relationship of a target and a collimation plate is studied and it came to complete this invention.

[0030] In order to attain the further purpose of this invention mentioned above, based on above-mentioned knowledge, the sputtering system concerning this invention It is made to make the target held at the target holder, and a target meet. In the sputtering system which is equipped with the wafer holder holding the wafer on which a target metal is made to deposit, and carries out sputtering of the target metal on a wafer It is characterized by making it intervene, where the collimation plate which consists of a conductor which has many through tubes penetrated towards the wafer between the target holder and the wafer holder from the target is grounded.

[0031] Moreover, the mediation effectiveness of a collimation plate changes sharply with locations to the target of a collimation plate, and there is criticality-meaning in the location to the target of a collimation plate about degradation prevention of the withstand voltage of gate oxide so that the result of the below-mentioned examples 1 and 2 of an experiment may show. So, at the suitable embodiment of this invention, a collimation plate is the 1st spacing D1 to a target electrode holder. It is the 2nd spacing D2 below. It is arranged at intervals of the above range, and the sputtering system is equipped with a justification means to position and hold a collimation plate in spacing of said range, still more suitably. the 1st spacing D1 and the 2nd spacing D2 -- the structure of a sputtering system -- moreover, the 1st spacing D1 although it differs, since it mentions later practical according to sputtering conditions, respectively 50mm -- it is -- the 2nd spacing D2 It is 24mm.

[0032] Moreover, although the higher one of the ratio of total of the opening area of all the through tubes to the surface area of a collimation plate and a numerical aperture is good and there is no constraint in the configuration and dimension of a through tube of a collimation plate, the aspect ratio of a through tube of a collimation plate is or more 0.7 1.3 or less reticular lamina suitably.

[0033] As long as it is the sputtering system which performs sputtering by glow discharge, there is no constraint in the class of sputtering system, and a format, and this invention can apply it at them, for example, can be applied to a direct-current sputtering system, a RF (RF) sputtering system, and magnetron sputtering equipment.

[0034] When a collimation plate intervenes between a target and a wafer, it is thought that it depends for extent of initial proof-pressure degradation of gate dielectric film on the aspect ratio and spatter rate of the distance of a collimation plate and a target holder and a collimation plate.

[0035] When a collimation plate does not intervene, the probability for the charged particle which comes flying from a high charged-particle field to collide with a wafer directly is high, therefore is as intense as a wafer periphery compared with a wafer center section. [of extent of initial proof-pressure degradation of the gate dielectric film of a wafer periphery] For example, since in the case of magnetron sputtering equipment the configuration of a cathode magnet differs from a dimension for every magnetron sputtering equipment, consequently the plasma density distribution of the target diameter direction as a result differs from distribution of a charged particle, although a degradation pattern (map) turns into a pattern peculiar to each equipment, degradation is as intense [a pattern] as a wafer periphery as a general inclination. Moreover, when a collimation plate does not intervene, it is clear that increase of the leakage current between the gate source / drain etc. is measured compared with the case where a collimation plate is made to intervene, and the damage is given to gate oxide also in the wafer center section at the time of a spatter.

[0036] As the distance (distance between traveler's checks) of a collimation plate and a target holder is the factor which should be determined that the probability which catches the charged particle which comes flying directly will become high and was mentioned above from this high charged-particle consistency region, the mediation effectiveness of a collimation plate changes sharply with locations to the target of a collimation plate, and there is criticality-meaning in the location to the target of a collimation plate. For example, the mediation effectiveness of a collimation plate falls sharply that the distance between traveler's checks is 50mm or more. If distance between traveler's checks is shortened and whenever [over the collimation plate of a charged particle / incident angle] is enlarged, since the prehension probability in the collimator plate of a charged particle can be raised, coming flying [of a charged particle] and degradation of the withstand voltage of the gate oxide by collision can be prevented effectively. However, if the distance between traveler's checks is too short, in order that a collimation plate may contact a high density plasma existence region conversely, there is a possibility that sputtering of the collimation plate may be carried out and it may be shaved, and since it is very dangerous, the permissible minimum distance (for example, 24mm) is set to the distance between traveler's checks from the standpoint.

[0037] Moreover, since the probability which catches the charged particle from the above-

mentioned high charged-particle consistency region becomes high, it is effective in degradation prevention of the initial withstand voltage of gate oxide to enlarge the aspect ratio of a collimation plate. However, if an aspect ratio is too large, since a spatter metal will be caught, a spatter rate falls.

[0038]

[Embodiment of the Invention] Next, the gestalt of each operation of this invention is explained with a drawing.

The 1st operation gestalt drawing 1 of the manufacture approach of the semiconductor device concerning this invention shows the component sectional view of each process of the gestalt of implementation of the 1st of the manufacture approach of the semiconductor device which becomes this invention. First, as shown in drawing 1 (a), the N well 102 is formed in the P type silicon substrate 101 by the known approach. Subsequently, field oxide 103 is formed in the front face of the P type silicon substrate 101 by the selective oxidation method as a field insulator layer. To the active region surrounded by this field oxide 103, gate dielectric film 104 and polycrystalline silicon, such as silicon oxide, are grown up one by one, Lynn is doped by known technique to polycrystalline silicon, and reduction of the electric resistance of polycrystalline silicon is aimed at.

[0039] Subsequently, as pattern NINGU of the polycrystalline silicon is carried out and it is shown in drawing 1 (a) by the photolithography method and the dry etching method which are known technique, the gate electrode 105 is formed. Next, the low-concentration N type impurity diffused layer 113 and the low-concentration P type impurity diffused layer 114 are formed with the photolithography method and ion-implantation. Subsequently, the sidewall 106 which consists of silicon oxide or a silicon nitride is formed in the side face of the gate electrode 105 using a known CVD technique and a known etching technique.

[0040] Next, as shown in drawing 1 (b), the source drain field 107 of an N type impurity diffused layer and the source drain field 108 of a P type impurity diffused layer are formed with the photolithography method and ion-implantation. In this way, the N type source drain field 107 and the P type source drain field 108 are formed as LDD structure.

[0041] Subsequently, the magnetron sputtering equipment made into conditions from which the amount Q of charges which removes the natural oxidation film of the front face of polycrystalline silicon and a semi-conductor substrate front face which is the gate electrode 105, for example, reaches the gate electrode 105 becomes two or less 5 C/cm is used, sputter deposition of the titanium which is a refractory metal is carried out, and the titanium film 109 is formed. Under the present circumstances, a reticulated conductor like a collimation plate is inserted between a wafer and a target, for example, and a spatter is performed to the magnetron sputtering equipment to be used.

[0042] Drawing 6 shows the block diagram of an example of the magnetron sputtering equipment used with the gestalt of operation of the 1st of this invention approach. a wafer 63 lays the magnetron sputtering equipment shown in drawing 6 (a) on the wafer holder 62 in a chamber 61 -- having -- this -- alienation -- the cathode magnet 64 and a target 65 are arranged in the location which counters, and the collimation plate 66 is arranged in the spatial position between a wafer 63 and a target 65.

[0043] Usually, although the collimation plate to be used raises the anisotropy of sputtered particles and the aspect ratio of a network is about one, the collimation plate 66 used with this sputtering system is a configuration which consists of a reticulated conductor, as a plan is shown in drawing 6 (b). In addition, that what is necessary is just to insert the plate which only has conductivity between a wafer and a target, this collimation plate 66 of the aspect ratio of the collimation plate 66 and a dimension, and a configuration is arbitrary, and the whole surface of a wafer 63 does not need to be covered, and or plasma intensity distribution are high, it should cover only the field which a charge tends to generate.

[0044] Furthermore, the configuration of this collimation plate 66 should just adjust a dimension and a configuration with a sputtering system again. In addition, although the reticulated conductor of this collimation plate 66 may be used as ********, corresponding to the plasma state, effectiveness goes up further by giving potential. Moreover, although the gestalt of the 1st

operation shows the example which deposited 109 for the titanium film, even if it makes it deposit other refractory metals, such as cobalt and nickel, of course, the same effectiveness is acquired.

[0045] Next, as shown in drawing 1 (c), the titanium silicide layer 110 of C49 mold structure is formed only in the interface of the titanium film 109 in contact with the front face of the gate electrode 105 and the source drain fields 107 and 108 which are polycrystalline silicon in a nitriding ambient atmosphere 700 degrees C or less by carrying out rapid heat treatment (RTA). Moreover, in this case, some of titanium film 109 in contact with field oxide 103 and a sidewall 106 and titanium film 109 on a semi-conductor substrate are nitrided, and it serves as the titanium nitride film 111.

[0046] Next, as shown in drawing 1 (d), by mixed liquor, such as aqueous ammonia and hydrogen peroxide solution, etc., wet etching is carried out alternatively and only unreacted titanium and the titanium nitride film 111 are removed. Subsequently, hot (800 degrees C or more) RTA is performed rather than the above-mentioned RTA, and the titanium silicide 112 of C54 mold structure where electrical resistivity is lower than the titanium silicide layer 110 of the aforementioned C49 mold structure is formed.

[0047] Thus, degradation of gate pressure-proofing according [the manufactured MOS mold field-effect transistor] to a spatter does not take place, but good gate pressure-proofing is obtained. Since the collimation plate 66 is inserted between the wafer 63 and the target 65, it is because the charge which should reach a wafer 63 flows to the collimation plate 66, the charge up of the gate electrode 105 is controlled and it is.

[0048] Thus, when carrying out sputter deposition of the refractory metal on a floating-gate electrode with the Salicide structure, a gate proof-pressure property can be raised by making the generated charge not reach a wafer as an approach of controlling the amount of charges which reaches to a wafer.

As shown in the 2nd operation gestalt drawing 2 (a) of the manufacture approach of the semiconductor device concerning this invention, the N well 202 is formed in the P type silicon substrate 201 by the known approach. Subsequently, field oxide 203 is formed in the front face of the P type silicon substrate 201 by the selective oxidation method as a field insulator layer. To the active region surrounded by this field oxide 203, gate dielectric film 204 and polycrystalline silicon, such as silicon oxide, are grown up one by one, Lynn is doped by known technique to polycrystalline silicon, and reduction of the electric resistance of polycrystalline silicon is aimed at. Subsequently, by the photolithography method and the dry etching method which are known technique, as shown in pattern NINGU drawing 2 (a), the gate electrode 205 is formed for polycrystalline silicon.

[0049] Next, the low-concentration N type impurity diffused layer 213 and the low-concentration P type impurity diffused layer 214 are formed with the photolithography method and ion-implantation. Subsequently, the sidewall 206 which consists of silicon oxide or a silicon nitride is formed in the side face of the gate electrode 205 using a known CVD technique and a known etching technique.

[0050] Next, as shown in drawing 2 (b), the source drain field 207 of an N type impurity diffused layer and the source drain field 208 of a P type impurity diffused layer are formed with the photolithography method and ion-implantation. Subsequently, the amount Q of charges which removes the natural oxidation film of the front face of polycrystalline silicon and a semi-conductor substrate front face which is the gate electrode 205, for example, reaches a gate electrode is 5 C/cm2. Using the magnetron sputtering equipment made into conditions which become below, sputter deposition of the titanium which is a refractory metal is carried out, and the titanium film 209 is formed.

[0051] The configuration of the magnetron sputtering equipment used at this time is shown in drawing 7 (b), (d), or (e). as a conventional sputtering system, as shown in drawing 7 (a), a wafer 73 lays on the wafer holder 72 in a chamber 71 -- having -- a wafer 73 -- alienation -- although the sputtering system of the structure without an electrode-holder magnet where the target 74 has been arranged in the location which counters was known, as for this thing, initial proof-pressure degradation of the gate was most seen for the field of max [consistency / of the

plasma 75 / plasma] by the experimental result with detailed artificers.
[0052] On the other hand, the magnetron sputtering equipment shown in drawing 7 (b) In the magnetron sputtering equipment of structure without an electrode-holder magnet So that the field of plasma consistency max of the plasma 77 may become a substrate (wafer) outside It was magnetron sputtering equipment of structure using the target 76 which set up magnitude, and since the charge generated from the plasma 77 was prevented from reaching a wafer 73 when sputter deposition of the above-mentioned titanium film 209 is carried out, the good electrical property was acquired.
[0053] Moreover, although the magnetron sputtering equipment shown in drawing 7 (a) and (b) is the structure where plasma 75 and 77 touches the wafer 73 directly, as shown in conventional magnetron sputtering equipment at drawing 7 (c), the magnetron sputtering equipment of the structure where it is equipped with the holder magnet 79 in the condition that the plasma 80 does not touch a wafer 73 is also known. That is, with this conventional magnetron sputtering equipment, the wafer 73 is laid through the holder magnet 79 on the wafer holder 72 in the chamber 71, and the plasma 80 from a target 74 does not touch a wafer 73.
[0054] However, also with this conventional magnetron sputtering equipment, when the charge (Ar+ or electron) generated from the plasma reached a wafer 73, the initial poor proof pressure of the gate arose similarly, and the degradation part of initial pressure-proofing of the gate was looked at by wafer 73 periphery from an artificer's detailed experimental result.
[0055] Then, the amount Q of charges which reaches a gate electrode in the titanium film 209 with the gestalt of this operation as magnetron sputtering equipment of structure with this electrode-holder magnet using the magnetron sputtering equipment of the structure shown in drawing 7 (d) or drawing 7 (e) is 5C/cm2. Sputter deposition is carried out on conditions which become below. the magnetron sputtering equipment equipment be show in drawing 7 (d) control the initial poor proof pressure of the gate by carry out the trap of the charge which the description be in the point which made the side face of a wafer 73 the wrap configuration, and generated by this the holder magnet 81 attach in order to stabilize a plasma from a plasma 82 by the magnetic field of the holder magnet 81.
[0056] moreover, the magnetron sputtering equipment show equipment in drawing 7 (e) have the description in the point of set up the magnetic field strength of the holder magnet 83 attach in order it stabilize a plasma as the plasma maximum field of a plasma 84 be above a wafer 83, and **** control the initial poor proof pressure of the gate by carry out the trap of the charge generate from a plasma 84 by the magnetic field of the holder magnet 83 by this.
[0057] In the case of the magnetron sputtering equipment of the structure shown in drawing 7 (d) or drawing 7 (e), by the trap of the charge having been carried out by the magnetic field generated from the holder magnets 81 and 83, the degradation part was not looked at by the periphery, either but the good electrical property was acquired. In fact, since extent of degradation of initial pressure-proofing of the gate changes with the structures of magnetron sputtering equipment, also when optimizing in the combination of the approach of changing the above-mentioned plasma maximum field, and the approach of carrying out a trap by the magnetic field generated with the holder magnet by the side of a wafer, it thinks.
[0058] Although the gestalt of this 2nd operation shows the example which deposited titanium, even if it makes it deposit other refractory metals, such as cobalt and nickel, of course, the same effectiveness is acquired.
[0059] The titanium silicide 210 of C49 mold structure is formed only in the interface of the titanium film 109 in contact with the front face of the gate electrode 205 and the source drain fields 107 and 108 which are polycrystalline silicon by carrying out rapid heat treatment (RTA) of 700 degrees C or less in nitrogen-gas-atmosphere mind next, for returning to drawing 2 again and explaining, as shown in drawing 2 (c). Moreover, in this case, as shown in drawing 2 (c), some of titanium film 209 in contact with field oxide 203 and a sidewall 206 and titanium film 209 on a semi-conductor substrate are nitrided, and it serves as the titanium nitride film 211.
[0060] Next, as shown in drawing 2 (d), by mixed liquor, such as aqueous ammonia and hydrogen peroxide solution, etc., wet etching is carried out alternatively and only unreacted titanium and the titanium nitride film 211 are removed. Subsequently, hot (800 degrees C or more) RTA is

performed rather than the above-mentioned RTA, and the titanium silicide 212 of low C54 mold structure of electrical resistivity is formed rather than the titanium silicide 210 of the aforementioned C49 mold structure.

[0061] With the gestalt of this operation, by making a magnetron sputtering equipment configuration into structure as shown in drawing 7 (b), (d), or (e), the charge generated from the plasma does not reach a wafer, but initial proof-pressure degradation of the gate is suppressed. Furthermore, since the reticulated collimation plate of a conductor is inserted with the magnetron sputtering equipment used with the gestalt of the 1st operation, When the film by which the spatter was carried out accumulates on the reticulated collimation plate of a conductor, a problems, such as a fall of the spatter rate to a wafer top, and particle, sake, With the magnetron sputtering equipment used with the gestalt of this 2nd operation to there being the need for exchange of a collimation plate, since the reticulated collimation plate of a conductor is not inserted, the need for exchange of a collimation plate is lost and there is also an advantage of being easy to maintain equipment to stability.

[0062] In addition, although the gestalt of the above the 1st and the 2nd operation showed how to form silicide on the gate and a diffusion layer at coincidence, of course, this invention is applicable also about the case where carry out the spatter of the refractory metal and silicide is formed on a diffusion layer on the floating gates, such as the polycide gate (WSix/Poly-Si), the PORITA mel gate (W/WNx/Poly-Si), or metal gate (W/SiO2) structure.

[0063] The example of the example book operation gestalt of an operation gestalt of the sputtering system concerning this invention is an example of the operation gestalt which applied the sputtering system concerning this invention to magnetron sputtering equipment, and the top view of a collimation plate and drawing 10 (c) of the typical sectional view in which drawing 10 (a) shows the configuration of the magnetron sputtering equipment of this example of an operation gestalt, and drawing 10 (b) are the side elevations of a collimation plate. The same sign is given to the same components as drawing 8 , and a part among drawing 10 . The magnetron sputtering equipment 30 of this example of an operation gestalt The wafer holder 14 which it has [holder] the configuration fundamentally same as shown in drawing 10 as the magnetron sputtering equipment shown in above-mentioned drawing 6 , and makes Wafer W lay in the spatter chamber 12, It has the collimation plate 32 of the shape of a wave plate established between the cathode magnet 16 which holds Target T in the location which estranges and meets to Wafer W, and the wafer holder 14 and the cathode magnet 16.

[0064] The collimation plate 32 is formed in order to catch a charged particle, while raising the anisotropy of sputtered particles, as shown in drawing 10 (b), is constituted as a reticular lamina which consists of a conductor of the network configuration which the forward hexagon was made to follow, and is grounded. Penetrating the mesh or hole of a forward hexagon of the collimation plate 32 toward Wafer W from Target T, the aspect ratio of a mesh or a hole is 1. That is, the path D (refer to a mesh or the overall diameter of a hole, and drawing 10 (b)) of thickness t (refer to drawing 10 (c)) of a collimation plate, a mesh, or a hole is the same die length. Moreover, according to the justification device 34, the distance (at the distance between traveler's checks and drawing 10 (a), it displays by L1) from the field of the collimation plate 32 to the target maintenance side of the cathode magnet 16 is changed, and the collimation plate 32 is held in the location. The justification device 34 is a known device and makes it go up and down the collimation plate 32 free up and down with driving gears, such as an oil hydraulic cylinder and an air cylinder. In addition, the collimation plate 32 does not need to cover the whole surface of Wafer W, plasma intensity distribution are high or the size of the collimation plate 32 should cover only the field which a charged particle tends to generate.

[0065] The sputtering experiment was conducted using the experimental device of the same configuration as the magnetron sputtering equipment 30 of this example of an operation gestalt which equipped the model number I-1060 made from example of experiment 1 Anelva with the collimation plate. Below, the specification of an experimental device is shown briefly. target thickness : 3mm diameter : 12 inch wafer holder wafer dimension: -- diameter [of 6 inch], or diameter chuck method [of 8 inch]: -- clamp chuck collimation plate aperture D : 23mm thickness t : Configuration of 23mm hole : continuation configuration aspect ratio [of a

forward hexagon]: -- the 1 quality of the material : Stainless steel [0066] With an above-mentioned experimental device, it is the distance (in the distance between T/S, and drawing 10 (a)) of the target maintenance side of the cathode magnet 16, and the front face of Wafer W. L2 a display -- 103mm -- adjusting -- and distance L1 of the target maintenance side of the cathode magnet 16, and the opposed face of the collimation plate 32 It is alike and adjusts to 34mm. The spatter power impressed between the wafer holder 14 and the cathode magnet 16 was changed into 1.0kW, 1.5kW, and 2.0kW, the spatter of the Co was carried out on the following sputtering conditions, and membranes were formed on the polish recon film which shows Co film of 100A of thickness to drawing 9 .

Sputtering condition holder temperature : Room-temperature chamber pressure: Three to 8 mTorr, subsequently to every chip, the quality of the withstand voltage of gate oxide was investigated, and as shown in drawing 12 (a) - (c), it painted for the chip of black and slight poor insulation to the chip of the serious poor insulation of gate oxide at gray.

[0067] The same experimental device as the example 1 of example of experiment 2 experiment is used, and it is the distance L2 of the target maintenance side of the cathode magnet 16, and the front face of Wafer W. It adjusts to 113mm. And distance L1 of the target maintenance side of the cathode magnet 16, and the opposed face of the collimation plate 32 24mm, The L1 [same / changing into 29mm, 34mm, 39mm, 44mm, and 56mm] The spatter power impressed between the wafer holder 14 and the cathode magnet 16 1.0kW, It changed into 1.5kW and 2.0kW, and Co sputtering was performed on conditions which are different in mutual [a total of 18 times of]. In addition, other conditions are the same as the same sputtering conditions as the example 1 of an experiment. Subsequently, as the quality of the withstand voltage of gate oxide was investigated for every chip and shown in drawing 13 (a) drawing 18 (a) - (c) from - (c), it painted for the chip of black and slight poor insulation to the chip of the serious poor insulation of gate oxide at gray.

[0068] As shown in drawing 19 , the experimental result of the examples 1 and 2 of an experiment was totaled by making spatter power into a parameter. drawing 1919 -- an axis of abscissa -- L1 -- the rate of an excellent article of gate oxide (%) is taken along the axis of ordinate. It is L1 irrespective of the size of spatter power as drawing 19 shows. In 39mm or less, the rate of an excellent article reaches to about 100%, and, on the other hand, it is L1. In 44mm or more, the rate of an excellent article falls to 60% or less rapidly. That is, it turns out about the rate of an excellent article of gate oxide, i.e., the mediation effectiveness of the collimation plate 32, that the clear critical-like location to the target or cathode magnet of the collimation plate 32 exists between 39mm and 44mm. The bar graph at the left end of drawing 19 is the numeric value of the rate of an excellent article at the time of not making a collimation plate intervene, and is L1. It is almost the same as the rate of an excellent article at the time of being 56mm.

[0069] Distance L1 of a collimation plate [as opposed to / use the same experimental device as the example 1 of example of experiment 3 experiment, and / a cathode magnet] Distance L2 of 29mm, a cathode magnet, and a wafer holder It was set as 68mm, the relation between spatter power (kW) and the rate of an excellent article of gate oxide was investigated under the following sputtering conditions, and the result was shown in drawing 20 . Moreover, for the comparison, using the magnetron sputtering equipment of the same configuration as a having-collimation plate ****** experimental device, sputtering was performed, the result was also doubled, and it was shown in drawing 20 .

Sputtering condition chamber pressure : 8 - 10mTorr quantity of gas flow : 100 [80 -] scc/m spatter power: Compared with the magnetron sputtering equipment which is not equipped with a collimation plate, the magnetron sputtering equipment of this example of an operation gestalt has the very low spatter power dependency of the rate of an excellent article of gate oxide by forming a collimation plate by the distance relation specified by this invention as 1.5kW drawing 20 shows.

[0070] Distance L1 of a collimation plate [as opposed to / use the same experimental device as the example 1 of example of experiment 4 experiment, and / a cathode magnet] Distance L2 of 29mm, a cathode magnet, and a wafer holder It was set as 68mm, the relation between a spatter rate (A/sec) and the rate of an excellent article of gate oxide was investigated under the

following sputtering conditions, and the result was displayed on drawing 21 . Moreover, for the comparison, using the magnetron sputtering equipment of the same configuration of the example of a having-collimation plate ******** operation gestalt, sputtering was performed, the result was also doubled, and it displayed on drawing 21 .
Sputtering condition chamber pressure : 8 - 10mTorr quantity of gas flow : 100 [80 -] scc/m spatter power: Compared with the magnetron sputtering equipment which is not equipped with a collimation plate, the magnetron sputtering equipment of this example of an operation gestalt has the low spatter rate dependency of the rate of an excellent article by forming a collimation plate by the distance relation specified by this invention as 1.5kW drawing 21 shows.
[0071] By the way, by raising a spatter rate, promptly, for a wrap reason, a charged particle comes to go to the horizontal direction of a wafer rather than the depth direction of the gate, and, as for the initial proof-pressure degradation probability of gate oxide, a conductive metal (or metal silicide) becomes low about a wafer front face. Therefore, it is effective in degradation prevention of the initial withstand voltage of gate oxide to raise a spatter rate, as shown in drawing 21 . However, if a spatter rate is too quick, in order for the field intima thickness distribution difference of a wafer to increase and to be further anxious about reduction of the silicide-ized reacting weight at the time of an elevated-temperature spatter etc., the spatter in a high spatter rate is not so desirable. Even when the spatter rate was raised by setting spatter power of the example 3 of an experiment to 2.6kW and distance [as opposed to the cathode maintenance side of the cathode magnet 16 for a collimation plate] was set to 50mm, it was verified that the rate of an excellent article is 98%. In addition, since the conductive metal membrane which intercepts flying to the gate of a charged particle is not formed immediately after a spatter starts even if it is going to raise a spatter rate and is going to aim at degradation prevention of the withstand voltage of gate oxide, compared with the case where a collimation plate is made to intervene, the effectiveness of initial proof-pressure degradation prevention of gate oxide is low. Moreover, the result it is satisfied with the result in en Jura (AMAT ENDURA) from which an equipment manufacturer differs of the result at least 46.5mm was obtained.
[0072] The magnetron sputtering equipment of this example of an operation gestalt used in the example 1 of example of experiment 5 experiment and the example 2 of an experiment is used. Distance L1 of the collimation plate to a cathode magnet 34mm, Distance L2 of a cathode magnet and a wafer holder Set it as 103mm, and fix applied voltage to 1.5kW, and gas pressure is set as 5mTorr(s), 8mmTorr, 10mTorr, and 15mTorr(s). Respectively, Co sputtering was performed and relation was investigated for the gas pressure dependency of the rate of an excellent article of gate oxide. Consequently, with the gas pressure of 5mTorr, 8mmTorr, 10mTorr, and 15mTorr (s), the rate of an excellent article of gate oxide is 100%, respectively, and it turned out that there is no gas pressure dependency in the rate of an excellent article of gate oxide with the magnetron sputtering equipment which formed the collimation plate.
[0073] From the result of the example 1 of an experiment to the above example 5 of an experiment, in case the sputtering system of this example of an operation gestalt form the refractory metal silicide film in a gate electrode by arrange the collimation plate 32 to the cathode maintenance side of the cathode magnet 16 in the range of 24mm or more 50mm or less distance, as degradation of the withstand voltage of gate oxide do not produce it, it be prove that it be the sputtering system which can carry out the spatter of the refractory metal on the polish recon film. Moreover, about the rate of an excellent article of gate oxide, the sputtering system of this example of an operation gestalt has a spatter power dependency, a spatter rate dependency, and a low gas pressure dependency, and can set up sputtering conditions in the large range.
[0074]
[Effect of the Invention] In the manufacture approach of the semiconductor device which forms a refractory metal silicide layer between the insulator layers alternatively formed on a semi-conductor substrate according to this invention as explained above In order to carry out sputter deposition of the refractory metal on the conditions which degradation of gate pressure-proofing does not produce, the case where the MOS mold field-effect transistor (MOSFET) which attains low resistance-ization by forming a refractory metal silicide layer is made detailed by thin-film-

izing and high integration of gate dielectric film -- more -- dependability -- it can manufacture highly.

[0075] According to the sputtering system concerning this invention, between a target holder and a wafer holder By making it intervene, where the collimation plate which consists of a conductor which has the through tube of a large number penetrated towards the wafer from the target is grounded, suitably It is the 1st spacing D1 to a target electrode holder about a collimation plate. It is the 2nd spacing D2 below. By arranging at intervals of the above range In case the refractory metal silicide film is formed in a gate electrode, as degradation of the withstand voltage of gate oxide did not arise, the sputtering system which can carry out the spatter of the refractory metal on the polish recon film is realized. Moreover, about the rate of an excellent article of gate oxide, the sputtering system concerning this invention has a spatter power dependency, a spatter rate dependency, and a low gas pressure dependency, and can set up sputtering conditions in the large range.

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TECHNICAL FIELD

[Field of the Invention] This invention relates to the manufacture approach of an MOS mold field-effect transistor (MOSFET) of attaining low resistance-ization, by starting the manufacture approach of a semiconductor device, especially silicide-izing the gate, the source, and a drain front face in self align. Moreover, in case this invention forms the refractory metal silicide film in a gate electrode, as degradation of the withstand voltage of gate oxide does not arise, it relates to the sputtering system which can carry out the spatter of the refractory metal on the polish recon film.

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PRIOR ART

[Description of the Prior Art] There is an approach indicated by JP,2-45923,A in the conventional salicide process known as one of the manufacture approaches of a semiconductor device. The manufacture approach of this conventional semiconductor device is explained with reference to drawing of longitudinal section shown in order of the process of drawing 3 (a) - drawing 3 (d).
[0003] As shown in drawing 3 (a), the N well 302 is formed in the P type silicon substrate 301 by the known approach. Subsequently, field oxide 303 is formed in the front face of the P type silicon substrate 301 by the selective oxidation method as a field insulator layer. To the active region surrounded by this field oxide 303, gate dielectric film 304 and polycrystalline silicon, such as silicon oxide, are grown up one by one, Lynn is doped by known technique to polycrystalline silicon, and reduction of the electric resistance of polycrystalline silicon is aimed at. Subsequently, by the photolithography method and the dry etching method which are known technique, pattern NINGU of the polycrystalline silicon is carried out, and the gate electrode 305 is formed.
[0004] Next, with the photolithography method and ion-implantation, as shown in drawing 3 (a), the low-concentration N type impurity diffused layer 313 and the low-concentration P type impurity diffused layer 314 are formed. Subsequently, the sidewall 306 which consists of silicon oxide or a silicon nitride is formed in the side face of the gate electrode 305 using a known chemical-vapor-deposition (CVD) technique and a known etching technique.
[0005] Next, as shown in drawing 3 (b), the N type impurity diffused layer 307 and the P type impurity diffused layer 308 are formed with the photolithography method and ion-implantation. In this way, the N type source drain field 307 and the P type source drain field 308 are formed as LDD structure. Subsequently, the natural oxidation film of the front face of polycrystalline silicon and a semi-conductor substrate front face which is a gate electrode is removed, for example, sputter deposition of the titanium film 309 is carried out.
[0006] Next, as shown in drawing 3 (c), only the titanium film 309 which contacts silicon in nitrogen-gas-atmosphere mind 700 degrees C or less by carrying out rapid heat treatment (following, RTA) is silicide-ized, and the titanium silicide layer 310 of C49 mold structure is formed. Moreover, in this case, some of titanium film 309 in contact with field oxide 303 and a sidewall 306 and titanium film on a semi-conductor substrate are nitrided, and it serves as the titanium nitride film 311.
[0007] Next, as shown in drawing 3 (d), by mixed liquor, such as aqueous ammonia and hydrogen peroxide solution, etc., wet etching is carried out alternatively and only unreacted titanium and the titanium nitride film 311 are removed. Subsequently, hot (800 degrees C or more) RTA is performed rather than the above-mentioned RTA, and the titanium silicide layer 312 of C54 mold structure where electrical resistivity is lower than the titanium silicide layer 310 of the aforementioned C49 mold structure is formed.
[0008] By using the salicide process shown above, since the surface parts of polycrystalline silicon 305, N type, and the P type impurity diffused layers 307 and 308 are silicide-ized in self align, low resistance is formed, and improvement in the speed of a device can be attained. This salicide process has the advantage which can carry out [silicide]-izing alternatively only within

the field to need.
[0009] By the way, generally, conventional magnetron sputtering equipment 10 equips with the cathode magnet 16 holding Target T the wafer holder 14 which makes Wafer W lay in the spatter chamber 12, and the location which estranges to Wafer W and meets it, as shown in drawing 8 . It had become a problem, when the chip which poor insulation produced in gate oxide was generated in generating on a wafer, especially a wafer periphery in many cases and the product yield was raised, in case the spatter of the Co was carried out and Co silicide electrode was formed on a polish recon gate electrode, using conventional magnetron sputtering equipment 10.
[0010] Here, using conventional magnetron sputtering equipment 10, the spatter of the Co is carried out on the polish recon of a gate electrode on the following spatter conditions, Co film is formed, and the result of having given RTA subsequently and having examined the quality of the withstand voltage of gate oxide for Co silicide-ization for every chip of a wafer after **** is shown. In an exam, using conventional magnetron sputtering equipment 10, as shown in drawing 9 , the spatter of the Co is carried out on the polish recon film 22 of the gate electrode formed on the silicon substrate 20, the Co film 24 is formed, subsequently RTA is given, and Co silicide layer is formed. Drawing 9 shows the condition of having formed the Co film 24 on the polish recon film 22 of a gate electrode by sputtering. The sidewall which 26 become from SiN etc., and 28 are gate oxide among drawing 9 .
Sputtering condition chamber pressure : 5 - 15mTorr quantity of gas flow Ar/50 - 100 scc/m spatter power : : In 1.5kW, however Co sputtering using conventional magnetron sputtering equipment 10 As shown in drawing 11 , especially to the gate oxide of the chip of the periphery of a wafer As poor insulation occurred and the withstand voltage of gate oxide showed the percentage to the chip of the whole wafer of the good chip beyond a predetermined value, and the so-called rate of an excellent article to drawing 19 together with the result of the example 1 of an experiment, and the example 2 of an experiment, it was about 46%. At drawing 11 , it is painted for the chip which poor insulation black [the chip which serious poor insulation has generated in gate oxide], and slight has generated in gray.

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EFFECT OF THE INVENTION

[Effect of the Invention] In the manufacture approach of the semiconductor device which forms a refractory metal silicide layer between the insulator layers alternatively formed on a semiconductor substrate according to this invention as explained above In order to carry out sputter deposition of the refractory metal on the conditions which degradation of gate pressure-proofing does not produce, the case where the MOS mold field-effect transistor (MOSFET) which attains low resistance-ization by forming a refractory metal silicide layer is made detailed by thin-film-izing and high integration of gate dielectric film -- more -- dependability -- it can manufacture highly.
[0075] According to the sputtering system concerning this invention, between a target holder and a wafer holder By making it intervene, where the collimation plate which consists of a conductor which has the through tube of a large number penetrated towards the wafer from the target is grounded, suitably It is the 1st spacing D1 to a target electrode holder about a collimation plate. It is the 2nd spacing D2 below. By arranging at intervals of the above range In case the refractory metal silicide film is formed in a gate electrode, as degradation of the withstand voltage of gate oxide did not arise, the sputtering system which can carry out the spatter of the refractory metal on the polish recon film is realized. Moreover, about the rate of an excellent article of gate oxide, the sputtering system concerning this invention has a spatter power dependency, a spatter rate dependency, and a low gas pressure dependency, and can set up sputtering conditions in the large range.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] However, by the manufacture approach of the above-mentioned conventional semiconductor device, after forming gate polish recon, when sputter deposition of the refractory metal was carried out on gate polish recon, on that occasion, the gate electrode 305 carried out the charge up with the charge generated from the plasma, and there was a problem that gate pressure-proofing deteriorated.
[0012] Although a salicide process is an effective approach as an approach of forming silicide only on a gate electrode and a diffusion layer, the natural oxidation film of the front face of the gate electrode 305 is removed for the substrate structure at the time of carrying out the spatter of the refractory metal, and, as for the gate electrode 305, an impurity is already doped, and it has become the floating gate.
[0013] Therefore, at the time of a spatter, a charge is generated in the gate polar zone at the moment of the shutter having opened from the discharge at the time during spatter discharge of standby, and sputter deposition being started especially, to a wafer, the charge flows gate dielectric film 304, and the problem that gate pressure-proofing deteriorates occurs. this phenomenon -- the thickness of gate dielectric film 304 -- thin-film-izing -- it is integrated highly -- it has been a serious problem as it is alike and it takes, and it is remarkable and detailed-ization progresses.
[0014] This invention was made in view of the above-mentioned point, and aims at offering the manufacture approach of the semiconductor device which carries out the spatter of the refractory metal on the conditions which degradation of the gate pressure-proofing by the sputtering system does not produce in the manufacture approach of the semiconductor device which forms a refractory metal silicide layer between the insulator layers alternatively formed on a semi-conductor substrate.
[0015] Moreover, other purposes of this invention are to offer the manufacture approach of a semiconductor device that high-reliability and the MOS mold field-effect transistor in which the reduction in resistance is possible can be manufactured.
[0016] Moreover, as mentioned above, when carrying out the spatter of the refractory metals, such as Co, Ti, nickel, and W, on the polish recon film and performing silicide-ization using conventional magnetron sputtering equipment, there was a problem that the insulation of gate oxide fell. Then, in case the further purpose of this invention forms the refractory metal silicide film in a gate electrode, it is offering the sputtering system which can carry out the spatter of the refractory metal on the polish recon film as degradation of the withstand voltage of gate oxide does not arise.

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MEANS

[Means for Solving the Problem] For this invention, the amount Q of charges which reaches a gate electrode in the manufacture approach of the semiconductor device which deposits a refractory metal all over the silicon substrate in which the gate electrode of a semiconductor device was formed in order to attain the above-mentioned purpose, heat-treats after forming the refractory metal film, and forms a refractory metal silicide layer in an interface with the refractory metal film is 5 C/cm2. It is the conditions which become the following and is made to carry out sputter deposition of the refractory metal film with magnetron sputtering equipment.
[0018] Here, above magnetron sputtering equipment is a configuration which sets up the magnitude of a target and carries out sputter deposition of the refractory metal so that the plasma consistency maximum field may become the outside of a silicon substrate.
[0019] Moreover, the configuration in which the holder magnet by the side of a silicon substrate carries out sputter deposition of the refractory metal for the wafer side face in which it has a silicon substrate, in the state of a wrap is sufficient as the above-mentioned magnetron sputtering equipment, and the configuration which sets up the reinforcement of the holder magnet by the side of a wafer, and carries out sputter deposition of the refractory metal is sufficient as it so that the field of plasma consistency max may become the upper part from the wafer which has a silicon substrate.
[0020] Furthermore, the configuration which carries out sputter deposition of the refractory metal where the collimation plate of a conductor is inserted in the space between a target and the wafer which has a silicon substrate is sufficient as above magnet RONSUPATTA equipment. In addition, as for the above-mentioned refractory metal, it is desirable that it is any 1 metal of titanium, cobalt, and nickel.
[0021] The amount Q of charges which reaches a gate electrode in this invention is 5 C/cm2. Sputter deposition of a refractory metal is performed on the conditions which become below, and it is made not to produce degradation of gate pressure-proofing.
[0022] An operation of this is explained. After drawing 4 etches the natural oxidation film using fluoric acid, it carries out sputter deposition of the titanium, and, subsequently shows the rate of an excellent article of gate pressure-proofing of the wafer which carried out wet etching of the deposited titanium by the mixed liquor of aqueous ammonia and hydrogen peroxide solution, without heat-treating. What was measured as a comparison, without performing a spatter is shown.
[0023] Since the poor initial proof pressure of the gate has happened and gate pressure-proofing deteriorates sharply during a spatter when the spatter of the titanium is carried out and it carries out wet etching immediately, the rate of a gate excellent article in that case has a low rate of an excellent article compared with the rate II of a gate excellent article when not carrying out the spatter of the titanium to drawing 4 , as I shows.
[0024] In case sputter deposition of drawing 5 is carried out, it shows the rate of a gate proof-pressure excellent article at the time of carrying out sputter deposition of the rate of a gate proof-pressure excellent article at the time of inserting a collimation plate between a wafer and a target without inserting a collimation plate, and the rate of a gate proof-pressure excellent article when not carrying out sputter deposition by comparison. Without performing a spatter

postheat treatment like drawing 4 also in this case, wet etching was carried out and it has measured.
[0025] It turns out that it is 100% like the rate V of a gate proof-pressure excellent article when not carrying out sputter deposition, and degradation of the gate pressure-proofing by the spatter does not take place compared with the rate of a gate proof-pressure excellent article as III shows, when the spatter of the titanium is carried out and it carries out wet etching to this drawing immediately, but good gate pressure-proofing is obtained as IV shows the rate of a gate proof-pressure excellent article at the time of inserting a collimation plate between a wafer and a target when carrying out sputter deposition to drawing 5 .
[0026] In this case, the amount Q of charges which the charge which should reach a wafer flows to a collimation plate since the collimation plate is inserted between the wafer and the target, the charge up of a gate electrode is controlled, and reaches a gate electrode is 5 C/cm2. It is because sputter deposition which becomes below is made.
[0027] Usually, a collimation spatter is for depositing titanium on the pars basilaris ossis occipitalis of a contact hole with a sufficient anisotropy, and improving the coverage of the spatter film. However, it is not necessary to carry out using an established collimation plate, and the result obtained using the collimation spatter and the same result are obtained in this case that the reticulated plate grounded electrically should just be inserted between the wafer and the target, for example.
[0028] Thus, when carrying out sputter deposition of the refractory metal on a floating-gate electrode with the Salicide structure, it is possible from the plasma whether make the generated charge whether make it not generate an unnecessary charge or not reach a wafer as an approach of controlling the amount of charges which reaches to a wafer. Therefore, a gate proof-pressure property can be raised by combining above-mentioned two kinds or them.
[0029] In order that this invention person might realize the sputtering system which can attain the purpose of this invention mentioned above, the cause which the poor insulation of gate oxide generates arrived at the wafer front face, and the charged particle near the target found it out after research, when it was in penetrating the polish recon film and gate oxide of a gate electrode, and intruding a silicon substrate. That is, it was surmised that the cause which degradation of the withstand voltage of gate oxide produces was because the probability of collision which a charged particle comes flying from the high charged-particle consistency field which exists near the plasma (wafer side), and collides with a wafer increases. The field where a plasma consistency is high is concentrated on the periphery rather than the center section about the diameter direction of a target so that clearly from the Heroux Gen measurement of a target. And although the field where a plasma consistency is high is seen in the direction which faces to a wafer from a target and it exists near the **** of a target, it is thought that the field where a charged-particle consistency is high exists in the wafer side of a plasma field rather. Then, in order that a charged particle may prevent coming flying on a wafer and colliding, it is a location near a target, the collimation plate has been arranged in the location moreover slightly separated from the plasma field to the wafer side, and it hit on an idea of catching a charged particle with a collimation plate, and further, the physical relationship of a target and a collimation plate is studied and it came to complete this invention.
[0030] In order to attain the further purpose of this invention mentioned above, based on above-mentioned knowledge, the sputtering system concerning this invention It is made to make the target held at the target holder, and a target meet. In the sputtering system which is equipped with the wafer holder holding the wafer on which a target metal is made to deposit, and carries out sputtering of the target metal on a wafer It is characterized by making it intervene, where the collimation plate which consists of a conductor which has many through tubes penetrated towards the wafer between the target holder and the wafer holder from the target is grounded.
[0031] Moreover, the mediation effectiveness of a collimation plate changes sharply with locations to the target of a collimation plate, and there is criticality-meaning in the location to the target of a collimation plate about degradation prevention of the withstand voltage of gate oxide so that the result of the below-mentioned examples 1 and 2 of an experiment may show. So, at the suitable embodiment of this invention, a collimation plate is the 1st spacing D1 to a

target electrode holder. It is the 2nd spacing D2 below. It is arranged at intervals of the above range, and the sputtering system is equipped with a justification means to position and hold a collimation plate in spacing of said range, still more suitably. the 1st spacing D1 and the 2nd spacing D2 -- the structure of a sputtering system -- moreover, the 1st spacing D1 although it differs, since it mentions later practical according to sputtering conditions, respectively 50mm -- it is -- the 2nd spacing D2 It is 24mm.

[0032] Moreover, although the higher one of the ratio of total of the opening area of all the through tubes to the surface area of a collimation plate and a numerical aperture is good and there is no constraint in the configuration and dimension of a through tube of a collimation plate, the aspect ratio of a through tube of a collimation plate is or more 0.7 1.3 or less reticular lamina suitably.

[0033] As long as it is the sputtering system which performs sputtering by glow discharge, there is no constraint in the class of sputtering system, and a format, and this invention can apply it at them, for example, can be applied to a direct-current sputtering system, a RF (RF) sputtering system, and magnetron sputtering equipment.

[0034] When a collimation plate intervenes between a target and a wafer, it is thought that it depends for extent of initial proof-pressure degradation of gate dielectric film on the aspect ratio and spatter rate of the distance of a collimation plate and a target holder and a collimation plate.

[0035] When a collimation plate does not intervene, the probability for the charged particle which comes flying from a high charged-particle field to collide with a wafer directly is high, therefore is as intense as a wafer periphery compared with a wafer center section. [of extent of initial proof-pressure degradation of the gate dielectric film of a wafer periphery] For example, since in the case of magnetron sputtering equipment the configuration of a cathode magnet differs from a dimension for every magnetron sputtering equipment, consequently the plasma density distribution of the target diameter direction as a result differs from distribution of a charged particle, although a degradation pattern (map) turns into a pattern peculiar to each equipment, degradation is as intense [a pattern] as a wafer periphery as a general inclination. Moreover, when a collimation plate does not intervene, it is clear that increase of the leakage current between the gate source / drain etc. is measured compared with the case where a collimation plate is made to intervene, and the damage is given to gate oxide also in the wafer center section at the time of a spatter.

[0036] As the distance (distance between traveler's checks) of a collimation plate and a target holder is the factor which should be determined that the probability which catches the charged particle which comes flying directly will become high and was mentioned above from this high charged-particle consistency region, the mediation effectiveness of a collimation plate changes sharply with locations to the target of a collimation plate, and there is criticality-meaning in the location to the target of a collimation plate. For example, the mediation effectiveness of a collimation plate falls sharply that the distance between traveler's checks is 50mm or more. If distance between traveler's checks is shortened and whenever [over the collimation plate of a charged particle / incident angle] is enlarged, since the prehension probability in the collimator plate of a charged particle can be raised, coming flying [of a charged particle] and degradation of the withstand voltage of the gate oxide by collision can be prevented effectively. However, if the distance between traveler's checks is too short, in order that a collimation plate may contact a high density plasma existence region conversely, there is a possibility that sputtering of the collimation plate may be carried out and it may be shaved, and since it is very dangerous, the permissible minimum distance (for example, 24mm) is set to the distance between traveler's checks from the standpoint.

[0037] Moreover, since the probability which catches the charged particle from the above-mentioned high charged-particle consistency region becomes high, it is effective in degradation prevention of the initial withstand voltage of gate oxide to enlarge the aspect ratio of a collimation plate. However, if an aspect ratio is too large, since a spatter metal will be caught, a spatter rate falls.

[0038]

[Embodiment of the Invention] Next, the gestalt of each operation of this invention is explained with a drawing.
The 1st operation gestalt drawing 1 of the manufacture approach of the semiconductor device concerning this invention shows the component sectional view of each process of the gestalt of implementation of the 1st of the manufacture approach of the semiconductor device which becomes this invention. First, as shown in drawing 1 (a), the N well 102 is formed in the P type silicon substrate 101 by the known approach. Subsequently, field oxide 103 is formed in the front face of the P type silicon substrate 101 by the selective oxidation method as a field insulator layer. To the active region surrounded by this field oxide 103, gate dielectric film 104 and polycrystalline silicon, such as silicon oxide, are grown up one by one, Lynn is doped by known technique to polycrystalline silicon, and reduction of the electric resistance of polycrystalline silicon is aimed at.
[0039] Subsequently, as pattern NINGU of the polycrystalline silicon is carried out and it is shown in drawing 1 (a) by the photolithography method and the dry etching method which are known technique, the gate electrode 105 is formed. Next, the low-concentration N type impurity diffused layer 113 and the low-concentration P type impurity diffused layer 114 are formed with the photolithography method and ion-implantation. Subsequently, the sidewall 106 which consists of silicon oxide or a silicon nitride is formed in the side face of the gate electrode 105 using a known CVD technique and a known etching technique.
[0040] Next, as shown in drawing 1 (b), the source drain field 107 of an N type impurity diffused layer and the source drain field 108 of a P type impurity diffused layer are formed with the photolithography method and ion-implantation. In this way, the N type source drain field 107 and the P type source drain field 108 are formed as LDD structure.
[0041] Subsequently, the magnetron sputtering equipment made into conditions from which the amount Q of charges which removes the natural oxidation film of the front face of polycrystalline silicon and a semi-conductor substrate front face which is the gate electrode 105, for example, reaches the gate electrode 105 becomes two or less 5 C/cm is used, sputter deposition of the titanium which is a refractory metal is carried out, and the titanium film 109 is formed. Under the present circumstances, a reticulated conductor like a collimation plate is inserted between a wafer and a target, for example, and a spatter is performed to the magnetron sputtering equipment to be used.
[0042] Drawing 6 shows the block diagram of an example of the magnetron sputtering equipment used with the gestalt of operation of the 1st of this invention approach. a wafer 63 lays the magnetron sputtering equipment shown in drawing 6 (a) on the wafer holder 62 in a chamber 61 -- having -- this -- alienation -- the cathode magnet 64 and a target 65 are arranged in the location which counters, and the collimation plate 66 is arranged in the spatial position between a wafer 63 and a target 65.
[0043] Usually, although the collimation plate to be used raises the anisotropy of sputtered particles and the aspect ratio of a network is about one, the collimation plate 66 used with this sputtering system is a configuration which consists of a reticulated conductor, as a plan is shown in drawing 6 (b). In addition, that what is necessary is just to insert the plate which only has conductivity between a wafer and a target, this collimation plate 66 of the aspect ratio of the collimation plate 66 and a dimension, and a configuration is arbitrary, and the whole surface of a wafer 63 does not need to be covered, and or plasma intensity distribution are high, it should cover only the field which a charge tends to generate.
[0044] Furthermore, the configuration of this collimation plate 66 should just adjust a dimension and a configuration with a sputtering system again. In addition, although the reticulated conductor of this collimation plate 66 may be used as ********, corresponding to the plasma state, effectiveness goes up further by giving potential. Moreover, although the gestalt of the 1st operation shows the example which deposited 109 for the titanium film, even if it makes it deposit other refractory metals, such as cobalt and nickel, of course, the same effectiveness is acquired.
[0045] Next, as shown in drawing 1 (c), the titanium silicide layer 110 of C49 mold structure is formed only in the interface of the titanium film 109 in contact with the front face of the gate

electrode 105 and the source drain fields 107 and 108 which are polycrystalline silicon in a nitriding ambient atmosphere 700 degrees C or less by carrying out rapid heat treatment (RTA). Moreover, in this case, some of titanium film 109 in contact with field oxide 103 and a sidewall 106 and titanium film 109 on a semi-conductor substrate are nitrided, and it serves as the titanium nitride film 111.

[0046] Next, as shown in drawing 1 (d), by mixed liquor, such as aqueous ammonia and hydrogen peroxide solution, etc., wet etching is carried out alternatively and only unreacted titanium and the titanium nitride film 111 are removed. Subsequently, hot (800 degrees C or more) RTA is performed rather than the above-mentioned RTA, and the titanium silicide 112 of C54 mold structure where electrical resistivity is lower than the titanium silicide layer 110 of the aforementioned C49 mold structure is formed.

[0047] Thus, degradation of gate pressure-proofing according [the manufactured MOS mold field-effect transistor] to a spatter does not take place, but good gate pressure-proofing is obtained. Since the collimation plate 66 is inserted between the wafer 63 and the target 65, it is because the charge which should reach a wafer 63 flows to the collimation plate 66, the charge up of the gate electrode 105 is controlled and it is.

[0048] Thus, when carrying out sputter deposition of the refractory metal on a floating-gate electrode with the Salicide structure, a gate proof-pressure property can be raised by making the generated charge not reach a wafer as an approach of controlling the amount of charges which reaches to a wafer.

As shown in the 2nd operation gestalt drawing 2 (a) of the manufacture approach of the semiconductor device concerning this invention, the N well 202 is formed in the P type silicon substrate 201 by the known approach. Subsequently, field oxide 203 is formed in the front face of the P type silicon substrate 201 by the selective oxidation method as a field insulator layer. To the active region surrounded by this field oxide 203, gate dielectric film 204 and polycrystalline silicon, such as silicon oxide, are grown up one by one, Lynn is doped by known technique to polycrystalline silicon, and reduction of the electric resistance of polycrystalline silicon is aimed at. Subsequently, by the photolithography method and the dry etching method which are known technique, as shown in pattern NINGU drawing 2 (a), the gate electrode 205 is formed for polycrystalline silicon.

[0049] Next, the low-concentration N type impurity diffused layer 213 and the low-concentration P type impurity diffused layer 214 are formed with the photolithography method and ion-implantation. Subsequently, the sidewall 206 which consists of silicon oxide or a silicon nitride is formed in the side face of the gate electrode 205 using a known CVD technique and a known etching technique.

[0050] Next, as shown in drawing 2 (b), the source drain field 207 of an N type impurity diffused layer and the source drain field 208 of a P type impurity diffused layer are formed with the photolithography method and ion-implantation. Subsequently, the amount Q of charges which removes the natural oxidation film of the front face of polycrystalline silicon and a semi-conductor substrate front face which is the gate electrode 205, for example, reaches a gate electrode is 5 C/cm2. Using the magnetron sputtering equipment made into conditions which become below, sputter deposition of the titanium which is a refractory metal is carried out, and the titanium film 209 is formed.

[0051] The configuration of the magnetron sputtering equipment used at this time is shown in drawing 7 (b), (d), or (e). as a conventional sputtering system, as shown in drawing 7 (a), a wafer 73 lays on the wafer holder 72 in a chamber 71 -- having -- a wafer 73 -- alienation -- although the sputtering system of the structure without an electrode-holder magnet where the target 74 has been arranged in the location which counters was known, as for this thing, initial proof-pressure degradation of the gate was most seen for the field of max [consistency / of the plasma 75 / plasma] by the experimental result with detailed artificers.

[0052] On the other hand, the magnetron sputtering equipment shown in drawing 7 (b) In the magnetron sputtering equipment of structure without an electrode-holder magnet So that the field of plasma consistency max of the plasma 77 may become a substrate (wafer) outside It was magnetron sputtering equipment of structure using the target 76 which set up magnitude, and

since the charge generated from the plasma 77 was prevented from reaching a wafer 73 when sputter deposition of the above-mentioned titanium film 209 is carried out, the good electrical property was acquired.

[0053] Moreover, although the magnetron sputtering equipment shown in drawing 7 (a) and (b) is the structure where plasma 75 and 77 touches the wafer 73 directly, as shown in conventional magnetron sputtering equipment at drawing 7 (c), the magnetron sputtering equipment of the structure where it is equipped with the holder magnet 79 in the condition that the plasma 80 does not touch a wafer 73 is also known. That is, with this conventional magnetron sputtering equipment, the wafer 73 is laid through the holder magnet 79 on the wafer holder 72 in the chamber 71, and the plasma 80 from a target 74 does not touch a wafer 73.

[0054] However, also with this conventional magnetron sputtering equipment, when the charge (Ar+ or electron) generated from the plasma reached a wafer 73, the initial poor proof pressure of the gate arose similarly, and the degradation part of initial pressure-proofing of the gate was looked at by wafer 73 periphery from an artificer's detailed experimental result.

[0055] Then, the amount Q of charges which reaches a gate electrode in the titanium film 209 with the gestalt of this operation as magnetron sputtering equipment of structure with this electrode-holder magnet using the magnetron sputtering equipment of the structure shown in drawing 7 (d) or drawing 7 (e) is 5C/cm2. Sputter deposition is carried out on conditions which become below. the magnetron sputtering equipment equipment be show in drawing 7 (d) control the initial poor proof pressure of the gate by carry out the trap of the charge which the description be in the point which made the side face of a wafer 73 the wrap configuration, and generated by this the holder magnet 81 attach in order to stabilize a plasma from a plasma 82 by the magnetic field of the holder magnet 81.

[0056] moreover, the magnetron sputtering equipment show equipment in drawing 7 (e) have the description in the point of set up the magnetic field strength of the holder magnet 83 attach in order it stabilize a plasma as the plasma maximum field of a plasma 84 be above a wafer 83, and **** control the initial poor proof pressure of the gate by carry out the trap of the charge generate from a plasma 84 by the magnetic field of the holder magnet 83 by this.

[0057] In the case of the magnetron sputtering equipment of the structure shown in drawing 7 (d) or drawing 7 (e), by the trap of the charge having been carried out by the magnetic field generated from the holder magnets 81 and 83, the degradation part was not looked at by the periphery, either but the good electrical property was acquired. In fact, since extent of degradation of initial pressure-proofing of the gate changes with the structures of magnetron sputtering equipment, also when optimizing in the combination of the approach of changing the above-mentioned plasma maximum field, and the approach of carrying out a trap by the magnetic field generated with the holder magnet by the side of a wafer, it thinks.

[0058] Although the gestalt of this 2nd operation shows the example which deposited titanium, even if it makes it deposit other refractory metals, such as cobalt and nickel, of course, the same effectiveness is acquired.

[0059] The titanium silicide 210 of C49 mold structure is formed only in the interface of the titanium film 109 in contact with the front face of the gate electrode 205 and the source drain fields 107 and 108 which are polycrystalline silicon by carrying out rapid heat treatment (RTA) of 700 degrees C or less in nitrogen-gas-atmosphere mind next, for returning to drawing 2 again and explaining, as shown in drawing 2 (c). Moreover, in this case, as shown in drawing 2 (c), some of titanium film 209 in contact with field oxide 203 and a sidewall 206 and titanium film 209 on a semi-conductor substrate are nitrided, and it serves as the titanium nitride film 211.

[0060] Next, as shown in drawing 2 (d), by mixed liquor, such as aqueous ammonia and hydrogen peroxide solution, etc., wet etching is carried out alternatively and only unreacted titanium and the titanium nitride film 211 are removed. Subsequently, hot (800 degrees C or more) RTA is performed rather than the above-mentioned RTA, and the titanium silicide 212 of low C54 mold structure of electrical resistivity is formed rather than the titanium silicide 210 of the aforementioned C49 mold structure.

[0061] With the gestalt of this operation, by making a magnetron sputtering equipment configuration into structure as shown in drawing 7 (b), (d), or (e), the charge generated from the

plasma does not reach a wafer, but initial proof-pressure degradation of the gate is suppressed. Furthermore, since the reticulated collimation plate of a conductor is inserted with the magnetron sputtering equipment used with the gestalt of the 1st operation, When the film by which the spatter was carried out accumulates on the reticulated collimation plate of a conductor, a problems, such as a fall of the spatter rate to a wafer top, and particle, sake, With the magnetron sputtering equipment used with the gestalt of this 2nd operation to there being the need for exchange of a collimation plate, since the reticulated collimation plate of a conductor is not inserted, the need for exchange of a collimation plate is lost and there is also an advantage of being easy to maintain equipment to stability.

[0062] In addition, although the gestalt of the above the 1st and the 2nd operation showed how to form silicide on the gate and a diffusion layer at coincidence, of course, this invention is applicable also about the case where carry out the spatter of the refractory metal and silicide is formed on a diffusion layer on the floating gates, such as the polycide gate (WSix/Poly-Si), the PORITA mel gate (W/WNx/Poly-Si), or metal gate (W/SiO2) structure.

[0063] The example of the example book operation gestalt of an operation gestalt of the sputtering system concerning this invention is an example of the operation gestalt which applied the sputtering system concerning this invention to magnetron sputtering equipment, and the top view of a collimation plate and drawing 10 (c) of the typical sectional view in which drawing 10 (a) shows the configuration of the magnetron sputtering equipment of this example of an operation gestalt, and drawing 10 (b) are the side elevations of a collimation plate. The same sign is given to the same components as drawing 8 , and a part among drawing 10 . The magnetron sputtering equipment 30 of this example of an operation gestalt The wafer holder 14 which it has [holder] the configuration fundamentally same as shown in drawing 10 as the magnetron sputtering equipment shown in above-mentioned drawing 6 , and makes Wafer W lay in the spatter chamber 12, It has the collimation plate 32 of the shape of a wave plate established between the cathode magnet 16 which holds Target T in the location which estranges and meets to Wafer W, and the wafer holder 14 and the cathode magnet 16.

[0064] The collimation plate 32 is formed in order to catch a charged particle, while raising the anisotropy of sputtered particles, as shown in drawing 10 (b), is constituted as a reticular lamina which consists of a conductor of the network configuration which the forward hexagon was made to follow, and is grounded. Penetrating the mesh or hole of a forward hexagon of the collimation plate 32 toward Wafer W from Target T, the aspect ratio of a mesh or a hole is 1. That is, the path D (refer to a mesh or the overall diameter of a hole, and drawing 10 (b)) of thickness t (refer to drawing 10 (c)) of a collimation plate, a mesh, or a hole is the same die length. Moreover, according to the justification device 34, the distance (at the distance between traveler's checks and drawing 10 (a), it displays by L1) from the field of the collimation plate 32 to the target maintenance side of the cathode magnet 16 is changed, and the collimation plate 32 is held in the location. The justification device 34 is a known device and makes it go up and down the collimation plate 32 free up and down with driving gears, such as an oil hydraulic cylinder and an air cylinder. In addition, the collimation plate 32 does not need to cover the whole surface of Wafer W, plasma intensity distribution are high or the size of the collimation plate 32 should cover only the field which a charged particle tends to generate.

[0065] The sputtering experiment was conducted using the experimental device of the same configuration as the magnetron sputtering equipment 30 of this example of an operation gestalt which equipped the model number I-1060 made from example of experiment 1 Anelva with the collimation plate. Below, the specification of an experimental device is shown briefly.

target thickness : 3mm diameter : 12 inch wafer holder wafer dimension: -- diameter [of 6 inch], or diameter chuck method [of 8 inch]: -- clamp chuck collimation plate aperture D : 23mm thickness t : Configuration of 23mm hole : continuation configuration aspect ratio [of a forward hexagon]: -- the 1 quality of the material : Stainless steel [0066] With an above-mentioned experimental device, it is the distance (in the distance between T/S, and drawing 10 (a)) of the target maintenance side of the cathode magnet 16, and the front face of Wafer W. L2 a display -- 103mm -- adjusting -- and distance L1 of the target maintenance side of the cathode magnet 16, and the opposed face of the collimation plate 32 It is alike and adjusts to

34mm. The spatter power impressed between the wafer holder 14 and the cathode magnet 16 was changed into 1.0kW, 1.5kW, and 2.0kW, the spatter of the Co was carried out on the following sputtering conditions, and membranes were formed on the polish recon film which shows Co film of 100A of thickness to drawing 9 .
Sputtering condition holder temperature : Room-temperature chamber pressure: Three to 8 mTorr, subsequently to every chip, the quality of the withstand voltage of gate oxide was investigated, and as shown in drawing 12 (a) - (c), it painted for the chip of black and slight poor insulation to the chip of the serious poor insulation of gate oxide at gray.
[0067] The same experimental device as the example 1 of example of experiment 2 experiment is used, and it is the distance L2 of the target maintenance side of the cathode magnet 16, and the front face of Wafer W. It adjusts to 113mm. And distance L1 of the target maintenance side of the cathode magnet 16, and the opposed face of the collimation plate 32 24mm, The L1 [same / changing into 29mm, 34mm, 39mm, 44mm, and 56mm] The spatter power impressed between the wafer holder 14 and the cathode magnet 16 1.0kW, It changed into 1.5kW and 2.0kW, and Co sputtering was performed on conditions which are different in mutual [a total of 18 times of]. In addition, other conditions are the same as the same sputtering conditions as the example 1 of an experiment. Subsequently, as the quality of the withstand voltage of gate oxide was investigated for every chip and shown in drawing 13 (a) drawing 18 (a) - (c) from - (c), it painted for the chip of black and slight poor insulation to the chip of the serious poor insulation of gate oxide at gray.

[0068] As shown in drawing 19 , the experimental result of the examples 1 and 2 of an experiment was totaled by making spatter power into a parameter. drawing 1919 -- an axis of abscissa -- L1 -- the rate of an excellent article of gate oxide (%) is taken along the axis of ordinate. It is L1 irrespective of the size of spatter power as drawing 19 shows. In 39mm or less, the rate of an excellent article reaches to about 100%, and, on the other hand, it is L1. In 44mm or more, the rate of an excellent article falls to 60% or less rapidly. That is, it turns out about the rate of an excellent article of gate oxide, i.e., the mediation effectiveness of the collimation plate 32, that the clear critical-like location to the target or cathode magnet of the collimation plate 32 exists between 39mm and 44mm. The bar graph at the left end of drawing 19 is the numeric value of the rate of an excellent article at the time of not making a collimation plate intervene, and is L1. It is almost the same as the rate of an excellent article at the time of being 56mm.
[0069] Distance L1 of a collimation plate [as opposed to / use the same experimental device as the example 1 of example of experiment 3 experiment, and / a cathode magnet] Distance L2 of 29mm, a cathode magnet, and a wafer holder It was set as 68mm, the relation between spatter power (kW) and the rate of an excellent article of gate oxide was investigated under the following sputtering conditions, and the result was shown in drawing 20 . Moreover, for the comparison, using the magnetron sputtering equipment of the same configuration as a having-collimation plate ****** experimental device, sputtering was performed, the result was also doubled, and it was shown in drawing 20 .
Sputtering condition chamber pressure : 8 - 10mTorr quantity of gas flow : 100 [80 -] scc/m spatter power: Compared with the magnetron sputtering equipment which is not equipped with a collimation plate, the magnetron sputtering equipment of this example of an operation gestalt has the very low spatter power dependency of the rate of an excellent article of gate oxide by forming a collimation plate by the distance relation specified by this invention as 1.5kW drawing 20 shows.
[0070] Distance L1 of a collimation plate [as opposed to / use the same experimental device as the example 1 of example of experiment 4 experiment, and / a cathode magnet] Distance L2 of 29mm, a cathode magnet, and a wafer holder It was set as 68mm, the relation between a spatter rate (A/sec) and the rate of an excellent article of gate oxide was investigated under the following sputtering conditions, and the result was displayed on drawing 21 . Moreover, for the comparison, using the magnetron sputtering equipment of the same configuration of the example of a having-collimation plate ******** operation gestalt, sputtering was performed, the result was also doubled, and it displayed on drawing 21 .
Sputtering condition chamber pressure : 8 - 10mTorr quantity of gas flow : 100 [80 -] scc/m

spatter power: Compared with the magnetron sputtering equipment which is not equipped with a collimation plate, the magnetron sputtering equipment of this example of an operation gestalt has the low spatter rate dependency of the rate of an excellent article by forming a collimation plate by the distance relation specified by this invention as 1.5kW drawing 21 shows.

[0071] By the way, by raising a spatter rate, promptly, for a wrap reason, a charged particle comes to go to the horizontal direction of a wafer rather than the depth direction of the gate, and, as for the initial proof-pressure degradation probability of gate oxide, a conductive metal (or metal silicide) becomes low about a wafer front face. Therefore, it is effective in degradation prevention of the initial withstand voltage of gate oxide to raise a spatter rate, as shown in drawing 21 . However, if a spatter rate is too quick, in order for the field intima thickness distribution difference of a wafer to increase and to be further anxious about reduction of the silicide-ized reacting weight at the time of an elevated-temperature spatter etc., the spatter in a high spatter rate is not so desirable. Even when the spatter rate was raised by setting spatter power of the example 3 of an experiment to 2.6kW and distance [as opposed to the cathode maintenance side of the cathode magnet 16 for a collimation plate] was set to 50mm, it was verified that the rate of an excellent article is 98%. In addition, since the conductive metal membrane which intercepts flying to the gate of a charged particle is not formed immediately after a spatter starts even if it is going to raise a spatter rate and is going to aim at degradation prevention of the withstand voltage of gate oxide, compared with the case where a collimation plate is made to intervene, the effectiveness of initial proof-pressure degradation prevention of gate oxide is low. Moreover, the result it is satisfied with the result in en Jura (AMAT ENDURA) from which an equipment manufacturer differs of the result at least 46.5mm was obtained.

[0072] The magnetron sputtering equipment of this example of an operation gestalt used in the example 1 of example of experiment 5 experiment and the example 2 of an experiment is used. Distance L1 of the collimation plate to a cathode magnet 34mm, Distance L2 of a cathode magnet and a wafer holder Set it as 103mm, and fix applied voltage to 1.5kW, and gas pressure is set as 5mTorr(s), 8mmTorr, 10mTorr, and 15mTorr(s). Respectively, Co sputtering was performed and relation was investigated for the gas pressure dependency of the rate of an excellent article of gate oxide. Consequently, with the gas pressure of 5mTorr, 8mmTorr, 10mTorr, and 15mTorr (s), the rate of an excellent article of gate oxide is 100%, respectively, and it turned out that there is no gas pressure dependency in the rate of an excellent article of gate oxide with the magnetron sputtering equipment which formed the collimation plate.

[0073] From the result of the example 1 of an experiment to the above example 5 of an experiment, in case the sputtering system of this example of an operation gestalt form the refractory metal silicide film in a gate electrode by arrange the collimation plate 32 to the cathode maintenance side of the cathode magnet 16 in the range of 24mm or more 50mm or less distance, as degradation of the withstand voltage of gate oxide do not produce it, it be prove that it be the sputtering system which can carry out the spatter of the refractory metal on the polish recon film. Moreover, about the rate of an excellent article of gate oxide, the sputtering system of this example of an operation gestalt has a spatter power dependency, a spatter rate dependency, and a low gas pressure dependency, and can set up sputtering conditions in the large range.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is a component sectional view in each process of the gestalt of operation of the 1st of this invention.
[Drawing 2] It is a component sectional view in each process of the gestalt of operation of the 2nd of this invention.
[Drawing 3] The component sectional view in each process of an example of the conventional approach.
[Drawing 4] It is drawing showing the rate of an excellent article of the gate pressure-proofing at the time of carrying out on the conventional spatter conditions etc.
[Drawing 5] It is drawing showing the rate of an excellent article of the gate proof-pressure property at the time of inserting a collimation plate etc.
[Drawing 6] It is the block diagram of the sputtering system used with the gestalt of operation of the 1st of this invention.
[Drawing 7] It is the block diagram of the sputtering system of each example used with the gestalt of operation of the 2nd of this invention, and the conventional sputtering system.
[Drawing 8] It is the mimetic diagram showing the configuration of the conventional sputtering system.
[Drawing 9] It is the explanatory view of silicide-izing.
[Drawing 10] The top view of a collimation plate and drawing 10 (c) of the mimetic diagram in which drawing 10 (a) shows the configuration of the sputtering system of the example of an operation gestalt, and drawing 10 (b) are the side elevations of a collimation plate.
[Drawing 11] It is the wafer map in which gate oxide degradation at the time of carrying out sputtering using the conventional sputtering system is shown.
[Drawing 12] Drawing 12 (a) - (c) is a wafer map in which gate oxide degradation at the time of carrying out a spatter under conditions which are mutually different using the sputtering system of this example of an operation gestalt, respectively is shown.
[Drawing 13] Drawing 13 (a) - (c) is a wafer map in which gate oxide degradation at the time of carrying out a spatter under conditions which are mutually different using the sputtering system of this example of an operation gestalt, respectively is shown.
[Drawing 14] Drawing 14 (a) - (c) is a wafer map in which gate oxide degradation at the time of carrying out a spatter under conditions which are mutually different using the sputtering system of this example of an operation gestalt, respectively is shown.
[Drawing 15] Drawing 15 (a) - (c) is a wafer map in which gate oxide degradation at the time of carrying out a spatter under conditions which are mutually different using the sputtering system of this example of an operation gestalt, respectively is shown.
[Drawing 16] Drawing 16 (a) - (c) is a wafer map in which gate oxide degradation at the time of carrying out a spatter under conditions which are mutually different using the sputtering system of this example of an operation gestalt, respectively is shown.
[Drawing 17] Drawing 17 (a) - (c) is a wafer map in which gate oxide degradation at the time of carrying out a spatter under conditions which are mutually different using the sputtering system of this example of an operation gestalt, respectively is shown.

[Drawing 18] Drawing 17 (a) - (c) is a wafer map in which gate oxide degradation at the time of carrying out a spatter under conditions which are mutually different using the sputtering system of this example of an operation gestalt, respectively is shown.
[Drawing 19] It is the graph which totaled the experimental result of the examples 1 and 2 of an experiment by making spatter power into a parameter.
[Drawing 20] It is the graph which shows the spatter power dependency of the rate of an excellent article.
[Drawing 21] It is the graph which shows the spatter rate dependency of the rate of an excellent article.
[Description of Notations]
10 The Conventional Sputtering System
12 Spatter Chamber
14 Wafer Holder
16 Cathode Magnet
20 Silicon Substrate
22 Polish Recon Film
24 Co Film
26 Sidewall
28 Gate Oxide
30 Sputtering System of Example of Operation Gestalt
32 Collimation Plate
34 Justification Device
61 71 Chamber
62 72 Wafer holder
63 73 Wafer
65, 74, 76 Target
66 Collimation Plate
75, 77, 80, 82, 84 Plasma
79, 81, 83 Holder magnet
101 201 P type silicon substrate
102 202 N well
103 203 Field oxide
104 204 Gate dielectric film
105 205 Gate electrode
106 206 Sidewall
107 207 N type source drain field
108 208 P type source drain field
109 209 Titanium film
110 210 Titanium silicide layer of C49 mold structure
111 211 Titanium nitride film
112 212 Titanium silicide layer of C54 mold structure
113 213 N type impurity diffused layer
114 214 P type impurity diffused layer

[Translation done.]

* NOTICES *

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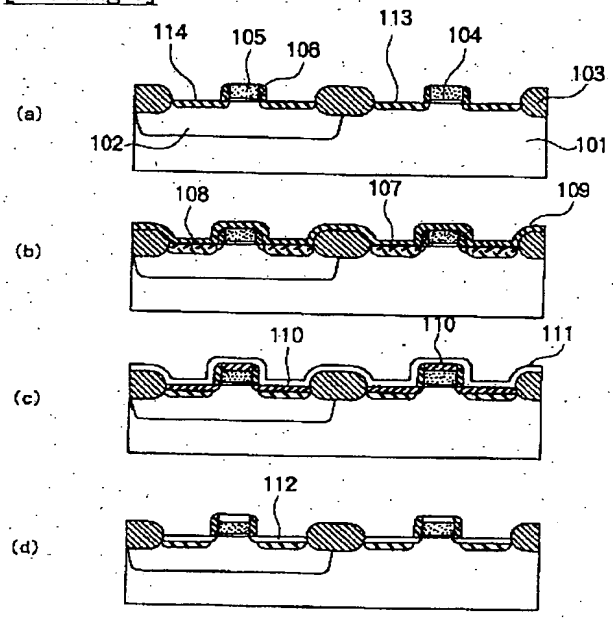
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

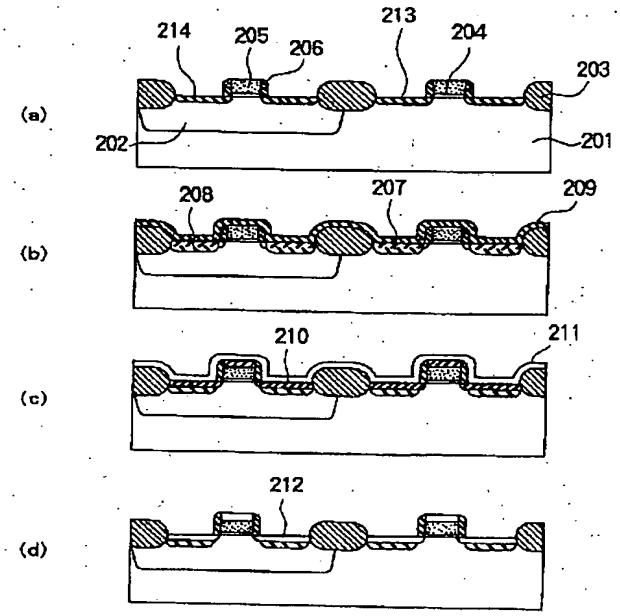
DRAWINGS

[Drawing 1]



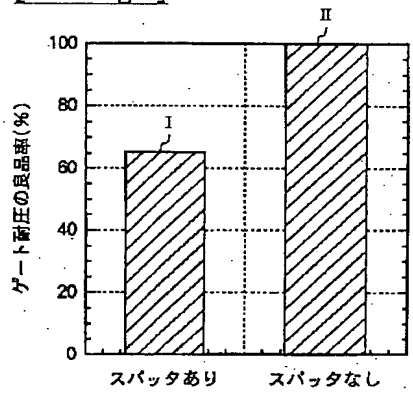
101 : P型シリコン基板　107 : N型ソース・ドレイン領域
102 : N型ウェル　108 : P型ソース・ドレイン領域
103 : フィールド酸化膜　109 : チタン膜
104 : ゲート絶縁膜　110 : C49型構造のチタンシリサイド層
105 : ゲート電極　111 : 窒化チタン膜
106 : サイドウォール　112 : C54構造のチタンシリサイド層

[Drawing 2]

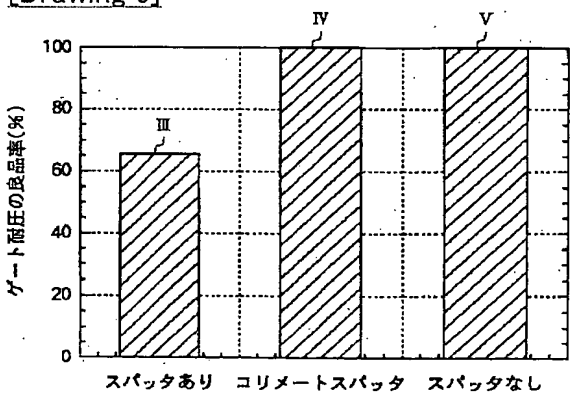


201 ：P型シリコン基板　207 ：N型ソース・ドレイン領域
202 ：N型ウェル　208 ：P型ソース・ドレイン領域
203 ：フィールド酸化膜　209 ：チタン膜
204 ：ゲート絶縁膜　210 ：C49型構造のチタンシリサイド層
205 ：ゲート電極　211 ：窒化チタン膜
206 ：サイドウォール　212 ：C54構造のチタンシリサイド層

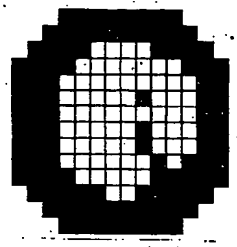
[Drawing 4]



[Drawing 5]

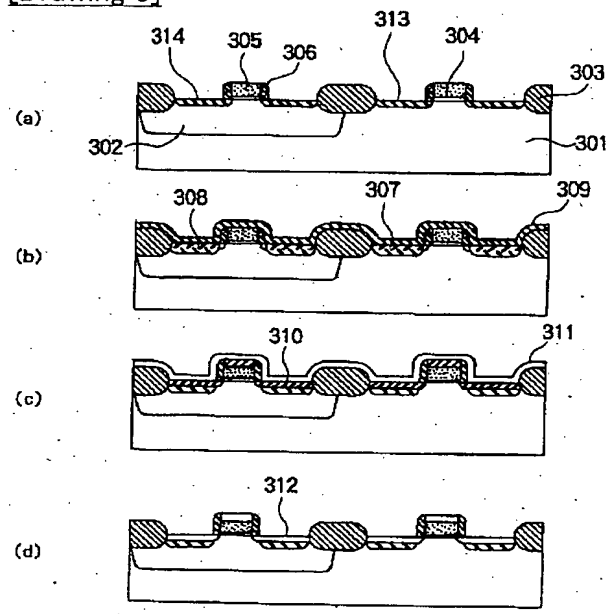


[Drawing 11]



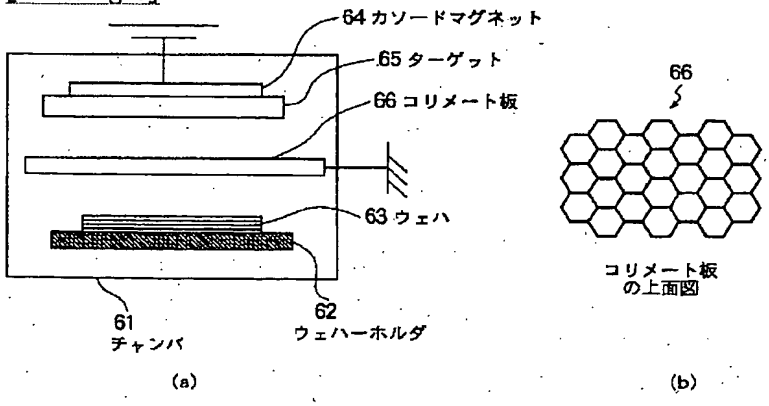
コリメータなし

[Drawing 3]

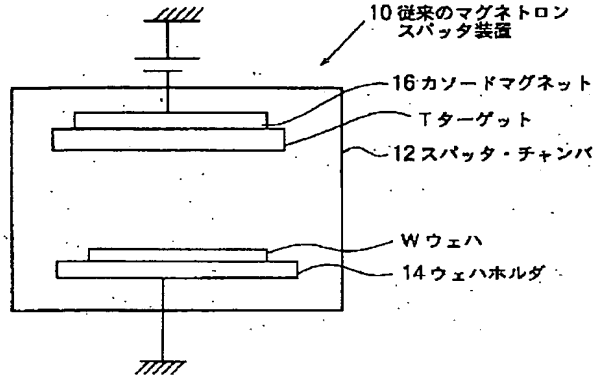


301 ：P型シリコン基板　307 ：N型ソース・ドレイン領域
302 ：N型ウェル　308 ：P型ソース・ドレイン領域
303 ：フィールド酸化膜　309 ：チタン膜
304 ：ゲート絶縁膜　310 ：C49型構造のチタンシリサイド層
305 ：ゲート電極　311 ：窒化チタン膜
306 ：サイドウォール　312 ：C54構造のチタンシリサイド層

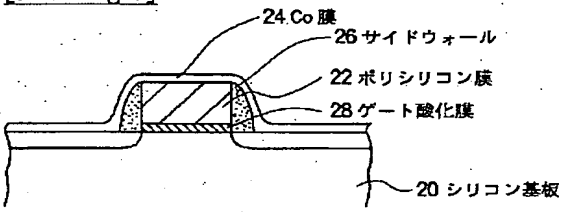
[Drawing 6]



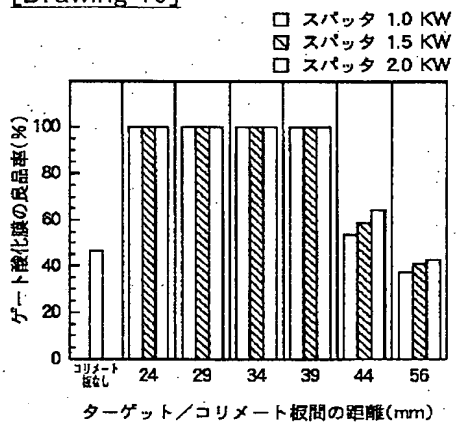
[Drawing 8]



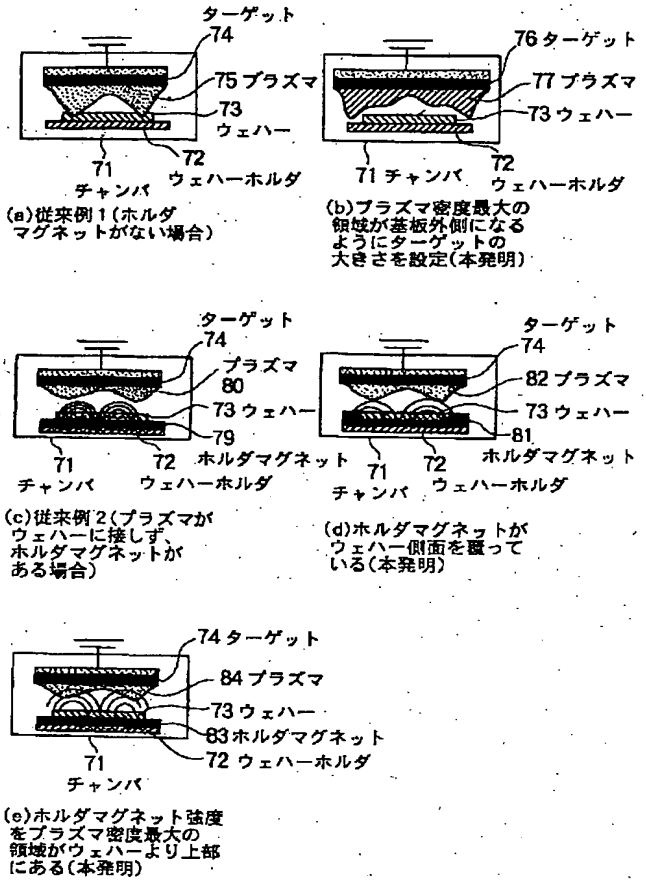
[Drawing 9]



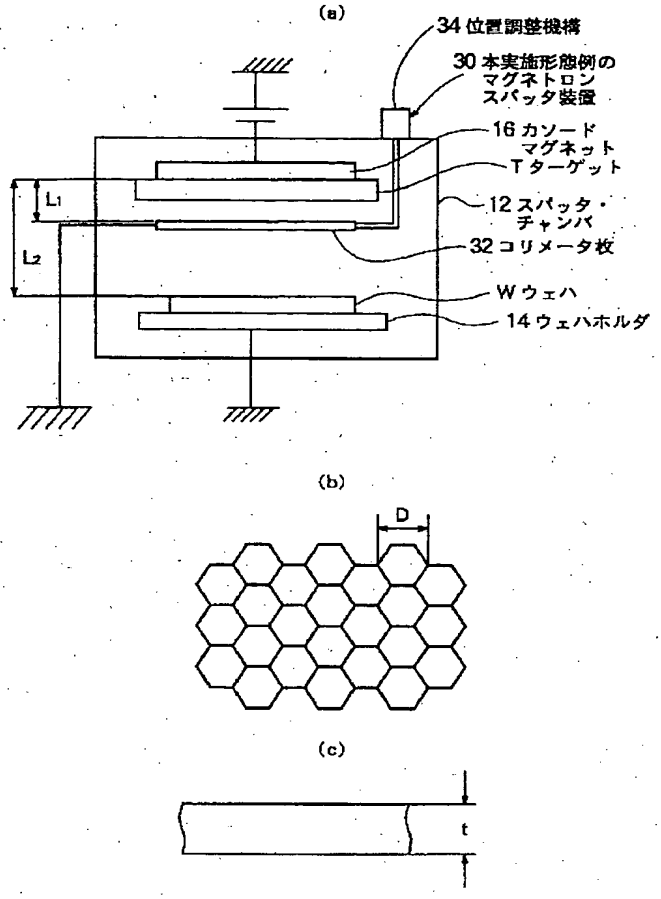
[Drawing 19]



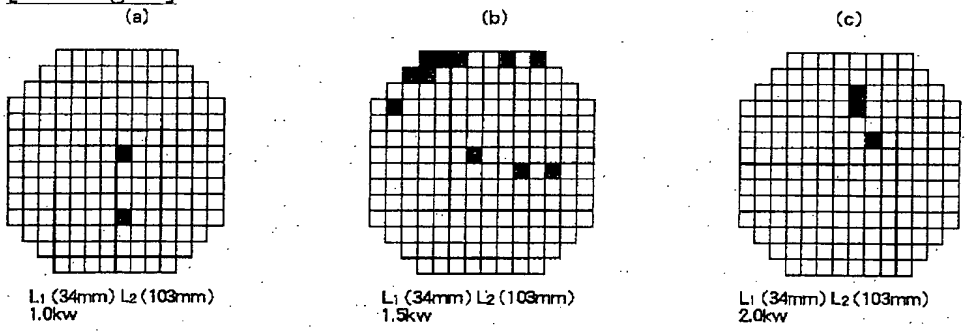
[Drawing 7]


ターゲット
74
75 プラズマ
73
ウェハー
72
ウェハーホルダ
71
チャンバ
(a)従来例1(ホルダ
マグネットがない場合)
76 ターゲット
77 プラズマ
73 ウェハー
72
ウェハーホルダ
71 チャンバ
(b)プラズマ密度最大の
領域が基板外側になる
ようにターゲットの
大きさを設定(本発明)
ターゲット
74
プラズマ
80
73 ウェハー
79
ホルダマグネット
71
チャンバ
72
ウェハーホルダ
(c)従来例2(プラズマが
ウェハーに接しず、
ホルダマグネットが
ある場合)
ターゲット
74
82 プラズマ
73 ウェハー
81
ホルダマグネット
71
チャンバ
72
ウェハーホルダ
(d)ホルダマグネットが
ウェハー側面を覆って
いる(本発明)
74 ターゲット
84 プラズマ
73 ウェハー
83 ホルダマグネット
72 ウェハーホルダ
71
チャンバ
(e)ホルダマグネット強度
をプラズマ密度最大の
領域がウェハーより上部
にある(本発明)

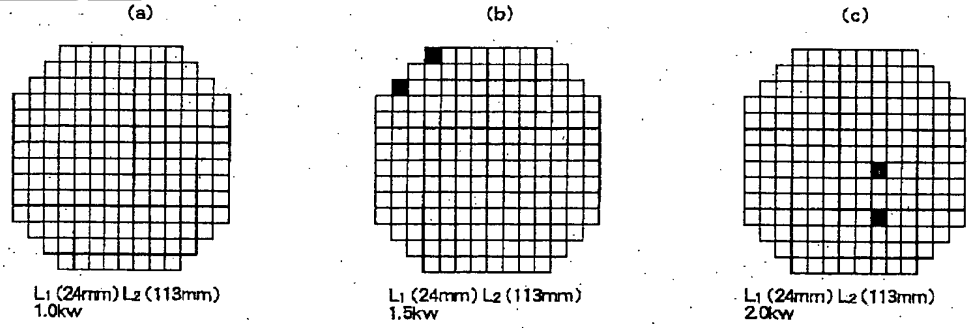
[Drawing 10]



[Drawing 12]

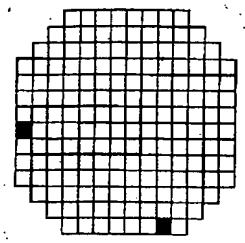


[Drawing 13]



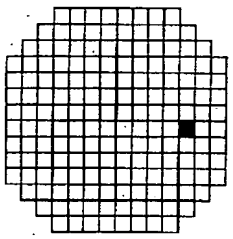
[Drawing 14]

(a)



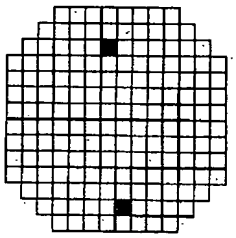
L1 (29mm) L2 (113mm)
1.0kw

(b)



L1 (29mm) L2 (113mm)
1.5kw

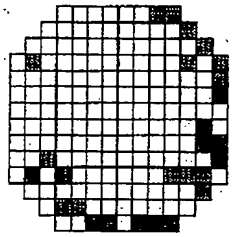
(c)



L1 (29mm) L2 (113mm)
2.0kw

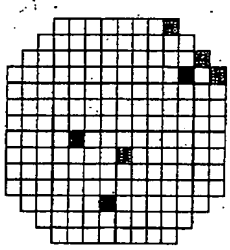
[Drawing 15]

(a)



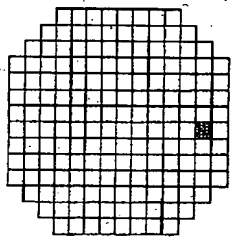
L1 (34mm) L2 (113mm)
1.0kw

(b)



L1 (34mm) L2 (113mm)
1.5kw

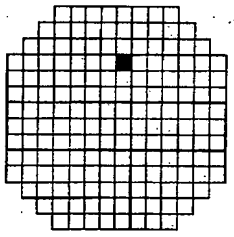
(c)



L1 (34mm) L2 (113mm)
2.0kw

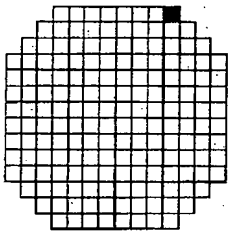
[Drawing 16]

(a)



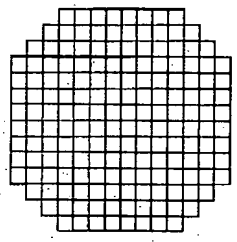
L1 (39mm) L2 (113mm)
1.0kw

(b)



L1 (39mm) L2 (113mm)
1.5kw

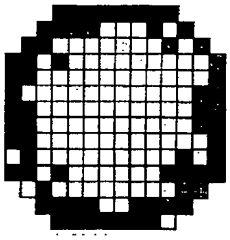
(c)



L1 (39mm) L2 (113mm)
2.0kw

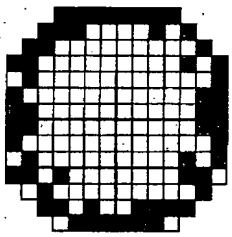
[Drawing 17]

(a)



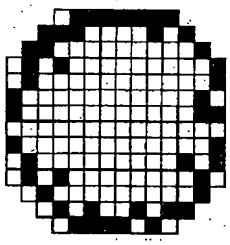
L1 (44mm) L2 (113mm)
1.0kw

(b)



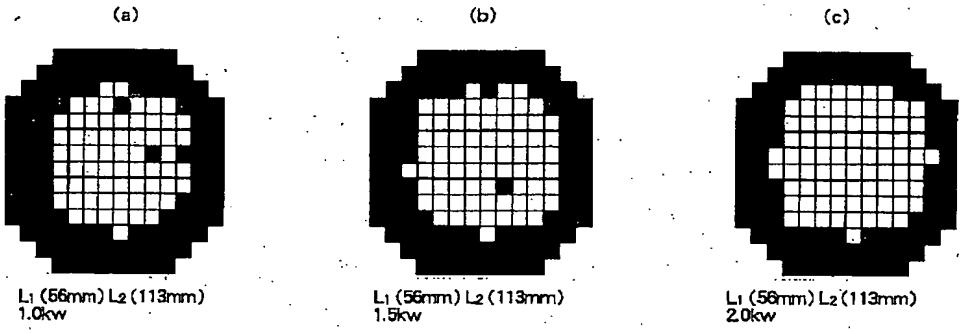
L1 (44mm) L2 (113mm)
1.5kw

(c)

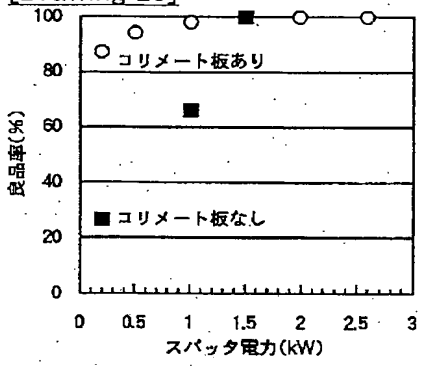


L1 (44mm) L2 (113mm)
2.0kw

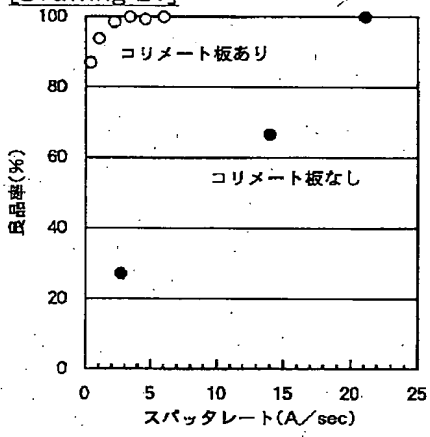
[Drawing 18]



[Drawing 20]



[Drawing 21]



[Translation done.]

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	３０１		３０１Ｒ
Ｃ２３Ｃ　14/34		Ｃ２３Ｃ　14/34	Ｒ
Ｈ０１Ｌ　21/8238		Ｈ０１Ｌ　27/08	３２１Ｆ
27/092		29/78	３０１Ｙ

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(22)出願日　平成10年(1998)９月２日

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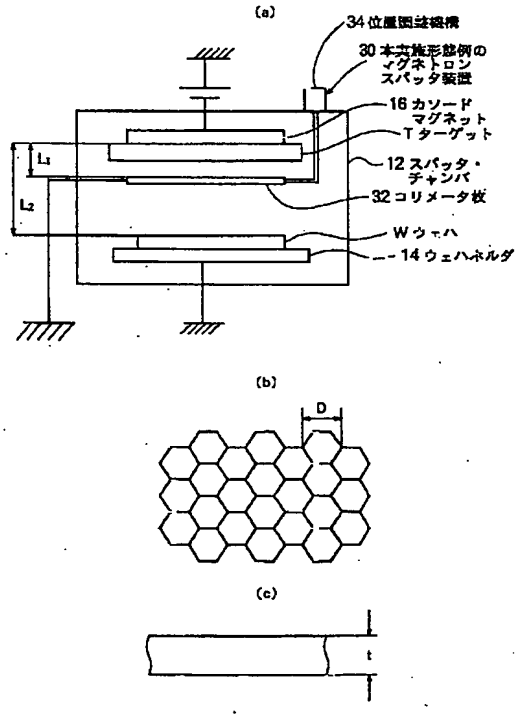
(54)【発明の名称】　半導体装置の製造方法及びスパッタ装置

(57)【要約】

【課題】　高融点金属シリサイド層を形成する半導体装置の製造方法において、スパッタ装置によるゲート耐圧の劣化が生じない条件で高融点金属をスパッタする半導体装置の製造方法及びそのためのスパッタ装置を提供する。

【解決手段】　本方法では、半導体素子のゲート電極が形成されたシリコン基板の全面に高融点金属を堆積して高融点金属膜を形成後、熱処理して高融点金属膜との界面に高融点金属シリサイド層を形成する際、ゲート電極に到達する電荷量Ｑが５Ｃ／ｃｍ^2 以下となる条件で、高融点金属膜をマグネトロンスパッタ装置によりスパッタ堆積する。また、スパッタ装置３０は、ターゲットホルダ１６と、ウェハーホルダ１４との間に、ターゲットからウェハーに向けて貫通した多数の貫通孔を有する導電体からなるコリメート板３２を接地した状態で有する。



【特許請求の範囲】
【請求項１】　半導体素子のゲート電極が形成されたシリコン基板の全面に高融点金属を堆積して高融点金属膜を形成後、熱処理して前記高融点金属膜との界面に高融点金属シリサイド層を形成する半導体装置の製造方法において、
前記ゲート電極に到達する電荷量Ｑが５Ｃ／ｃｍ² 以下となる条件で、前記高融点金属膜をマグネトロンスパッタ装置によりスパッタ堆積することを特徴とする半導体装置の製造方法。
【請求項２】　前記マグネトロンスパッタ装置は、プラズマ密度最大領域が前記シリコン基板の外側になるように、ターゲットの大きさを設定して前記高融点金属膜をスパッタ堆積する構成であることを特徴とする請求項１記載の半導体装置の製造方法。
【請求項３】　前記マグネトロンスパッタ装置は、前記シリコン基板側のホルダマグネットが該シリコン基板を有するウェハー側面を覆う状態で前記高融点金属をスパッタ堆積する構成であることを特徴とする請求項１記載の半導体装置の製造方法。
【請求項４】　前記マグネトロンスパッタ装置は、プラズマ密度最大の領域が前記シリコン基板を有するウェハーより上方になるように、該ウェハー側のホルダマグネットの強度を設定して前記高融点金属をスパッタ堆積する構成であることを特徴とする請求項１記載の半導体装置の製造方法。
【請求項５】　前記マグネトロンスパッタ装置は、ターゲットと前記シリコン基板を有するウェハーとの間の空間に、導電体のコリメート板を挿入した状態で前記高融点金属をスパッタ堆積する構成であることを特徴とする請求項１記載の半導体装置の製造方法。
【請求項６】　前記コリメート板は、上面の形状が網状であることを特徴とする請求項５記載の半導体装置の製造方法。
【請求項７】前記高融点金属は、チタン、コバルトおよびニッケルのいずれか一の金属であることを特徴とする請求項１乃至６のうちいずれか一項記載の半導体装置の製造方法。
【請求項８】　ターゲットホルダに保持されたターゲットと、ターゲットに対面させるようにして、ターゲット金属を堆積させるウェハーを保持するウェハーホルダとを備え、ターゲット金属をウェハー上にスパッタリングするスパッタ装置において、
ターゲットホルダと、ウェハーホルダとの間に、ターゲットからウェハーに向けて貫通した多数個の貫通孔を有する導電体からなるコリメート板を接地した状態で介在させることを特徴とするスパッタ装置。
【請求項９】　コリメート板が、ターゲットホルダーに対して第１の間隔D_1 以下で第２の間隔D_2 以上の範囲の間隔で配置されていることを特徴とする請求項８に記載のスパッタ装置。
【請求項１０】　第１の間隔D_1 が５０㎜であり、第２の間隔D_2 が２４㎜であることを特徴とする請求項１０に記載のスパッタ装置。
【請求項１１】　コリメート板を前記範囲の間隔内に位置決めし、保持する位置調整手段を備えていることを特徴とする請求項９又は１０に記載のスパッタ装置。
【請求項１２】　コリメート板は、貫通孔のアスペクト比が０．７以上で１．３以下の網状板であることを特徴とする請求項８から１１のうちのいずれか１項に記載のスパッタ装置。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、半導体装置の製造方法に係り、特にゲート、ソースおよびドレイン表面を自己整合的にシリサイド化することにより、低抵抗化を図るＭＯＳ型電界効果トランジスタ（ＭＯＳＦＥＴ）の製造方法に関する。また、本発明は、ゲート電極に高融点金属シリサイド膜を形成する際、ゲート酸化膜の絶縁耐圧の劣化が生じないようにして、高融点金属をポリシリコン膜上にスパッタできるスパッタ装置に関するものである。
【０００２】
【従来の技術】半導体装置の製造方法の一つとして知られる従来のサリサイドプロセスでは、特開平２－４５９２３号公報に開示された方法がある。この従来の半導体装置の製造方法について、図３（ａ）～図３（ｄ）の工程順に示した縦断面図を参照して説明する。
【０００３】図３（ａ）に示すようにＰ型シリコン基板３０１にＮウェル３０２を既知の方法により形成する。次いで、Ｐ型シリコン基板３０１の表面にフィールド絶縁膜としてフィールド酸化膜３０３を選択酸化法により形成する。このフィールド酸化膜３０３に囲まれた活性領域に、順次シリコン酸化膜などのゲート絶縁膜３０４と多結晶シリコンを成長し、多結晶シリコンにリンを既知の手法によりドープして多結晶シリコンの電気抵抗の低減を図る。次いで、既知の手法であるフォトリソグラフィー法とドライエッチング法により、多結晶シリコンをパターンニングしてゲート電極３０５を形成する。
【０００４】次に、フォトリソグラフィー法とイオン注入法により、図３（ａ）に示すように低濃度のＮ型不純物拡散層３１３と低濃度のＰ型不純物拡散層３１４を形成する。次いで、ゲート電極３０５の側面にシリコン酸化膜あるいはシリコン窒化膜から構成されるサイドウォール３０６を既知の化学気相成長（ＣＶＤ）技術とエッチング技術を用いて形成する。
【０００５】次に、図３（ｂ）に示すようにフォトリソグラフィー法とイオン注入法により、Ｎ型不純物拡散層３０７とＰ型不純物拡散層３０８を形成する。かくして、ＬＤＤ構造としてＮ型ソース・ドレイン領域３０

７、Ｐ型ソース・ドレイン領域３０８が形成される。次いで、ゲート電極である多結晶シリコンの表面と半導体基板表面の自然酸化膜を除去し、例えばチタン膜３０９をスパッタ堆積する。

【０００６】次に、図３（ｃ）に示すように窒素雰囲気中で７００℃以下の急速熱処理（以下、ＲＴＡ）することにより、シリコンと接触するチタン膜３０９のみをシリサイド化し、Ｃ４９型構造のチタンシリサイド層３１０を形成する。また、この際、フィールド酸化膜３０３およびサイドウォール３０６と接触するチタン膜３０９と半導体基板上のチタン膜の一部は窒化されて窒化チタン膜３１１となる。

【０００７】次に、図３（ｄ）に示すようにアンモニア水および過酸化水素水等の混合液などにより、選択的にウエットエッチングし、未反応チタンと窒化チタン膜３１１のみを除去する。次いで、前述のＲＴＡよりも高温（８００℃以上）のＲＴＡを行い、前記のＣ４９型構造のチタンシリサイド層３１０よりも電気抵抗率の低いＣ５４型構造のチタンシリサイド層３１２を形成する。

【０００８】以上に示したサリサイドプロセスを用いることにより、多結晶シリコン３０５、Ｎ型およびＰ型不純物拡散層３０７、３０８の表面部分が自己整合的にシリサイド化されるために低抵抗化され、デバイスの高速化が図れる。このサリサイドプロセスは、必要とする領域に限って、選択的にシリサイド化できる利点がある。

【０００９】ところで、従来のマグネトロンスパッタ装置１０は、一般的には、図８に示すように、スパッタ・チャンバ１２内に、ウェハーＷを載置させるウェハーホルダ１４と、ウェハーＷに離間して対面する位置にターゲットＴを保持するカソードマグネット１６とを備えている。従来のマグネトロンスパッタ装置１０を使って、例えばポリシリコンゲート電極上にＣｏをスパッタして、Ｃｏシリサイド電極を形成する際、ゲート酸化膜に絶縁不良が生じたチップが、ウェハー上に発生すること、特にウェハー周辺部に発生することが多く、製品歩留りを向上させる上で、問題になっていた。

【００１０】ここで、従来のマグネトロンスパッタ装置１０を使って、以下のスパッタ条件でゲート電極のポリシリコン上にＣｏをスパッタしてＣｏ膜を成膜し、次いでＲＴＡを施してＣｏシリサイド化を行っ後、ゲート酸化膜の絶縁耐圧の良否をウェハーのチップ毎に試験した結果を示す。本試験では、従来のマグネトロンスパッタ装置１０を使って、図９に示すように、シリコン基板２０上に形成されたゲート電極のポリシリコン膜２２上にＣｏをスパッタしてＣｏ膜２４を成膜し、次いでＲＴＡを施してＣｏシリサイド層を形成する。図９は、スパッタリングによりＣｏ膜２４をゲート電極のポリシリコン膜２２上に成膜した状態を示す。図９中、２６はＳｉＮ等からなるサイドウォール、２８はゲート酸化膜である。

スパッタリング条件
チャンバ圧力　：５～１５mTorr
ガス流量　　：Ａｒ／５０～１００scc/m
スパッタパワー：１．５ｋＷ

しかし、従来のマグネトロンスパッタ装置１０を使ったＣｏスパッタリングでは、図１１に示すように、特にウェハーの周辺部のチップのゲート酸化膜に、絶縁不良が発生し、ゲート酸化膜の絶縁耐圧が所定値以上の良好なチップのウェハー全体のチップに対する百分率、いわゆる良品率は、図１９に実験例１と実験例２の結果と合わせ示すように、４６％程度であった。図１１では、ゲート酸化膜に重度の絶縁不良が発生しているチップは、黒色で、軽度の絶縁不良が発生しているチップは、灰色で彩色されている。

【００１１】

【発明が解決しようとする課題】しかるに、上記の従来の半導体装置の製造方法では、ゲートポリシリコンを形成した後、ゲートポリシリコン上に高融点金属をスパッタ堆積すると、その際に、プラズマから発生する電荷によりゲート電極３０５がチャージアップし、ゲート耐圧が劣化するという問題があった。

【００１２】ゲート電極および拡散層上のみにシリサイドを形成する方法として、サリサイドプロセスが有効な方法であるが、高融点金属をスパッタする際の下地構造は、ゲート電極３０５の表面の自然酸化膜は除去されており、ゲート電極３０５は既に不純物がドープされてかつ、フローティングゲートとなっている。

【００１３】そのため、スパッタ時、特にスパッタ放電中あるいは待機時の放電からシャッターが開いてウェハーへスパッタ堆積が開始された瞬間にゲート電極部に電荷が発生し、その電荷がゲート絶縁膜３０４を流れて、ゲート耐圧が劣化するという問題が発生する。この現象は、ゲート絶縁膜３０４の膜厚が薄膜化や高集積化するにつれて顕著であり、微細化が進むにつれて深刻な問題となっている。

【００１４】本発明は上記の点に鑑みなされたもので、半導体基板上に選択的に形成される絶縁膜間に高融点金属シリサイド層を形成する半導体装置の製造方法において、スパッタ装置によるゲート耐圧の劣化が生じない条件で高融点金属をスパッタする半導体装置の製造方法を提供することを目的とする。

【００１５】また、本発明の他の目的は、高信頼性及び低抵抗化が可能なＭＯＳ型電界効果トランジスタを製造し得る半導体装置の製造方法を提供することにある。

【００１６】また、前述したように、従来のマグネトロンスパッタ装置を使って、Ｃｏ、Ｔｉ、Ｎｉ、Ｗ等の高融点金属をポリシリコン膜上にスパッタしてシリサイド化を施す際に、ゲート酸化膜の絶縁性が低下するという問題があった。そこで、本発明の更なる目的は、ゲート電極に高融点金属シリサイド膜を形成する際、ゲート酸

化膜の絶縁耐圧の劣化が生じないようにして、高融点金属をポリシリコン膜上にスパッタできるスパッタ装置を提供することである。

【００１７】

【課題を解決するための手段】本発明は、上記の目的を達成するため半導体素子のゲート電極が形成されたシリコン基板の全面に高融点金属を堆積して高融点金属膜を形成後、熱処理して高融点金属膜との界面に高融点金属シリサイド層を形成する半導体装置の製造方法において、ゲート電極に到達する電荷量Ｑが５Ｃ／ｃｍ^2 以下となる条件で、高融点金属膜をマグネトロンスパッタ装置によりスパッタ堆積するようにしたものである。

【００１８】ここで、上記のマグネトロンスパッタ装置は、プラズマ密度最大領域がシリコン基板の外側になるように、ターゲットの大きさを設定して高融点金属をスパッタ堆積する構成である。

【００１９】また、上記マグネトロンスパッタ装置は、シリコン基板側のホルダマグネットがシリコン基板を有するウェハー側面を覆う状態で高融点金属をスパッタ堆積する構成でもよく、またプラズマ密度最大の領域がシリコン基板を有するウェハーより上方になるように、ウェハー側のホルダマグネットの強度を設定して高融点金属をスパッタ堆積する構成でもよい。

【００２０】更に、上記のマグネットロンスパッタ装置は、ターゲットとシリコン基板を有するウェハーとの間の空間に、導電体のコリメート板を挿入した状態で高融点金属をスパッタ堆積する構成でもよい。なお、上記の高融点金属は、チタン、コバルトおよびニッケルのいずれか一の金属であることが望ましい。

【００２１】本発明では、ゲート電極に到達する電荷量Ｑが５Ｃ／ｃｍ^2 以下になる条件で高融点金属のスパッタ堆積を行い、ゲート耐圧の劣化を生じさせないようにするものである。

【００２２】このことの作用について説明する。図４は自然酸化膜をフッ酸を用いてエッチングした後、チタンをスパッタ堆積し、次いで、熱処理を行わずにアンモニア水と過酸化水素水の混合液により、堆積したチタンをウエットエッチングしたウェハーのゲート耐圧の良品率を示す。比較として、スパッタを行わずに測定したものも示してある。

【００２３】チタンをスパッタし、すぐにウェットエッチングした場合はゲートの初期耐圧不良が起こっており、スパッタ中にゲート耐圧が大幅に劣化するため、その場合のゲート良品率は図４にＩで示すように、チタンをスパッタしない場合のゲート良品率ＩＩに比べて良品率が低い。

【００２４】図５はスパッタ堆積する際、コリメート板をウェハーとターゲット間に挿入した場合のゲート耐圧良品率を、コリメート板を挿入しないでスパッタ堆積した場合のゲート耐圧良品率と、スパッタ堆積しない場合のゲート耐圧良品率とを対比して示す。この場合も図４と同様にスパッタ後熱処理を行わずにウェットエッチングし測定している。

【００２５】スパッタ堆積する際、コリメート板をウェハーとターゲット間に挿入した場合のゲート耐圧良品率は図５にIVで示す如く、スパッタ堆積しない場合のゲート耐圧良品率Ｖと同様１００％であり、同図にIIIで示すようにチタンをスパッタし、すぐにウェットエッチングした場合のゲート耐圧良品率に比べて、スパッタによるゲート耐圧の劣化が起こっておらず、良好なゲート耐圧が得られていることがわかる。

【００２６】この場合には、コリメート板がウェハーとターゲット間に挿入されているためにウェハーに到達するはずの電荷がコリメート板に流れて、ゲート電極のチャージアップが抑制されており、ゲート電極に到達する電荷量Ｑが５Ｃ／ｃｍ^2 以下になるようなスパッタ堆積ができるためである。

【００２７】通常コリメートスパッタは、コンタクトホールの底部にチタンを異方性良く堆積し、スパッタ膜のカバレッジを改善するためのものである。しかし、この場合においては、既成のコリメート板を用いて行わなくてもよく、電気的にアースされている例えば網状の板をウェハーとターゲットの間に挿入されていればよく、コリメートスパッタを用いて得られた結果と同様の結果が得られる。

【００２８】このように、サリサイド構造を有したフローティングゲート電極上に高融点金属をスパッタ堆積する場合には、ウェハーへ到達する電荷量を制御する方法として、プラズマから不要な電荷を発生しないようにするか、発生した電荷をウェハーに到達しないようにするかが考えられる。そのため、上述の２種類あるいはそれらを組み合わせることでゲート耐圧特性を向上させることができる。

【００２９】本発明者は、上述した本発明の目的を達成できるスパッタ装置を実現するために、研究の末に、ゲート酸化膜の絶縁不良が発生する原因は、ターゲット近傍の荷電粒子が、ウェハー表面に到達し、ゲート電極のポリシリコン膜及びゲート酸化膜を貫通してシリコン基板に貫入することにあると見い出した。即ち、ゲート酸化膜の絶縁耐圧の劣化が生じる原因は、プラズマ近傍（ウェハー側）に存在する高荷電粒子密度領域から荷電粒子が飛来してウェハーに衝突する衝突確率が増大するからであると推測した。ターゲットのエロージェン測定から明らかなように、プラズマ密度の高い領域は、ターゲットの直径方向について、中央部よりも周辺部に集中している。そして、プラズマ密度の高い領域は、ターゲットからウェハーに向かう方向に見て、ターゲットの極く近傍に存在するが、荷電粒子密度の高い領域は、むしろプラズマ領域のウェハー側に存在していると考えられる。そこで、荷電粒子が、ウェハー上に飛来し、衝突す

るのを防止するために、ターゲットに近い位置であって、しかもプラズマ領域から僅かにウェハー側に離れた位置にコリメート板を配置して、荷電粒子をコリメート板により捕捉することを着想し、更には、ターゲットとコリメート板との位置関係を研究して、本発明を完成するに到った。

【００３０】上述した本発明の更なる目的を達成するために、上述の知見に基づいて、本発明に係るスパッタ装置は、ターゲットホルダに保持されたターゲットと、ターゲットに対面させるようにして、ターゲット金属を堆積させるウェハーを保持するウェハーホルダとを備え、ターゲット金属をウェハー上にスパッタリングするスパッタ装置において、ターゲットホルダと、ウェハーホルダとの間に、ターゲットからウェハーに向けて貫通した多数個の貫通孔を有する導電体からなるコリメート板を接地した状態で介在させることを特徴としている。

【００３１】また、後述の実験例１及び２の結果から判るように、コリメート板の介在効果は、コリメート板のターゲットに対する位置によって大幅に異なり、ゲート酸化膜の絶縁耐圧の劣化防止に関し、コリメート板のターゲットに対する位置には、臨界的な意義がある。そこで、本発明の好適な実施態様では、コリメート板が、ターゲットホルダーに対して第１の間隔D_1 以下で第２の間隔D_2 以上の範囲の間隔で配置されていて、更に好適には、スパッタ装置は、コリメート板を前記範囲の間隔内に位置決めし、保持する位置調整手段を備えている。第１の間隔D_1 及び第２の間隔D_2は、スパッタ装置の構造により、またスパッタリング条件により、それぞれ、異なるものの、実用的には、後述する理由から、第１の間隔D_1 が５０㎜であり、第２の間隔D_2 が２４㎜である。

【００３２】また、コリメート板の表面積に対する全貫通孔の開口面積の総和の比率、開口率は高い方がよく、また、コリメート板の貫通孔の形状及び寸法に制約はないものの、好適には、コリメート板は、貫通孔のアスペクト比が０．７以上１．３以下の網状板である。

【００３３】本発明は、グロー放電によりスパッタリングを行うスパッタ装置である限り、スパッタ装置の種類、形式に制約はなく適用でき、例えば、直流スパッタ装置、高周波（ＲＦ）スパッタ装置及びマグネトロンスパッタ装置に適用できる。

【００３４】コリメート板がターゲットとウェハーとの間に介在する場合、ゲート絶縁膜の初期耐圧劣化の程度は、コリメート板とターゲットホルダとの距離、コリメート板のアスペクト比及びスパッタレートに依存すると考えられる。

【００３５】コリメート板が介在しない場合、高荷電粒子領域から飛来する荷電粒子が直接的にウェハーに衝突する確率は、ウェハー周辺部ほど高く、従ってウェハ周辺部のゲート絶縁膜の初期耐圧劣化の程度がウェハー中央部に比べて激しい。例えばマグネトロンスパッタ装置の場合、マグネトロンスパッタ装置毎にカソードマグネットの形状、寸法が異なり、その結果、ターゲット直径方向のプラズマ密度分布、ひいては荷電粒子の分布が異なるため、劣化パターン（マップ）は、各装置に固有なパターンとなるものの、一般的な傾向として、ウェハー周辺部ほど劣化が激しい。また、コリメート板が介在しない場合、ウェハ中央部でも、コリメート板を介在させた場合に比べて、ゲート・ソース／ドレイン間のリーク電流の増大などが計測されており、スパッタ時にゲート酸化膜にダメージが与えられていることは明らかである。

【００３６】コリメート板とターゲットホルダとの距離（Ｔ／Ｃ間距離）は、この高荷電粒子密度域から直接飛来する荷電粒子を捕捉する確率が高くなるように決定されるべき因子であって、前述したように、コリメート板の介在効果は、コリメート板のターゲットに対する位置によって大幅に異なり、コリメート板のターゲットに対する位置には臨界的な意義がある。例えば、Ｔ／Ｃ間距離が５０㎜以上であると、コリメート板の介在効果は大幅に低下する。Ｔ／Ｃ間距離を短くして、荷電粒子のコリメート板に対する入射角度を大きくすれば、荷電粒子のコリメータ板での捕捉確率を高めることができるので、荷電粒子の飛来、衝突によるゲート酸化膜の絶縁耐圧の劣化を効果的に防止できる。しかし、逆に、Ｔ／Ｃ間距離が短すぎると、高密度プラズマ存在領域にコリメート板が接触するために、コリメート板がスパッタリングされて削られる恐れがあり、非常に危険であるから、その見地からＴ／Ｃ間距離には許容最短距離（例えば２４㎜）が設定される。

【００３７】また、コリメート板のアスペクト比を大きくすることは、前述の高荷電粒子密度域からの荷電粒子を捕捉する確率が高くなるので、ゲート酸化膜の初期絶縁耐圧の劣化防止に有効である。しかし、アスペクト比が大きすぎると、スパッタ金属が捕捉されるので、スパッタレートが低下する。

【００３８】

【発明の実施の形態】次に本発明の各実施の形態について、図面と共に説明する。

本発明に係る半導体装置の製造方法の第１の実施形態

図１は本発明になる半導体装置の製造方法の第１の実施の形態の各工程の素子断面図を示す。まず、図１（ａ）に示すようにＰ型シリコン基板１０１にＮウェル１０２を既知の方法により形成する。次いで、Ｐ型シリコン基板１０１の表面にフィールド絶縁膜としてフィールド酸化膜１０３を選択酸化法により形成する。このフィールド酸化膜１０３に囲まれた活性領域に、順次シリコン酸化膜などのゲート絶縁膜１０４と多結晶シリコンを成長し、多結晶シリコンにリンを既知の手法によりドープして多結晶シリコンの電気抵抗の低減を図る。

【００３９】次いで、既知の手法であるフォトリソグラフィー法とドライエッチング法により、多結晶シリコンをパターンニングして図１（ａ）に示すようにゲート電極１０５を形成する。次に、フォトリソグラフィー法とイオン注入法により、低濃度のＮ型不純物拡散層１１３と低濃度のＰ型不純物拡散層１１４を形成する。次いで、ゲート電極１０５の側面にシリコン酸化膜あるいはシリコン窒化膜から構成されるサイドウォール１０６を既知のＣＶＤ技術とエッチング技術を用いて形成する。

【００４０】次に、図１（ｂ）に示すように、フォトリソグラフィー法とイオン注入法により、Ｎ型不純物拡散層のソース・ドレイン領域１０７とＰ型不純物拡散層のソース・ドレイン領域１０８を形成する。かくして、ＬＤＤ構造としてＮ型ソース・ドレイン領域１０７、Ｐ型ソース・ドレイン領域１０８が形成される。

【００４１】次いで、ゲート電極１０５である多結晶シリコンの表面と半導体基板表面の自然酸化膜を除去し、例えばゲート電極１０５に到達する電荷量Ｑが５Ｃ／ｃｍ^{2}以下になるような条件とするマグネトロンスパッタ装置を使用して、高融点金属であるチタンをスパッタ堆積してチタン膜１０９を形成する。この際、使用するマグネトロンスパッタ装置には、ウェハーとターゲット間にコリメート板のような例えば網状の導電体を挿入してスパッタを行う。

【００４２】図６は本発明方法の第１の実施の形態で使用するマグネトロンスパッタ装置の一例の構成図を示す。図６（ａ）に示すマグネトロンスパッタ装置は、チャンバ６１内にウェハーホルダ６２上にウェハー６３が載置され、これに離間対向する位置にカソードマグネット６４とターゲット６５が配置され、ウェハー６３とターゲット６５との間の空間位置にコリメート板６６が配置されている。

【００４３】通常用いるコリメート板は、スパッタ粒子の異方性を高めるものであり、網のアスペクト比が１程度のものであるが、このスパッタ装置で用いるコリメート板６６は、図６（ｂ）に上面図を示すように、網状の導電体からなる構成である。なお、このコリメート板６６は、単に導電性のある板をウェハーとターゲット間に挿入すればよく、コリメート板６６のアスペクト比および寸法、形状は任意であり、また、ウェハー６３の全面を覆っている必要もなく、プラズマ強度分布が高いあるいは電荷が発生しやすい領域だけをカバーしていればよい。

【００４４】さらに、また、このコリメート板６６の形状はスパッタ装置によって寸法、形状を調整すればいいものである。なお、このコリメート板６６の網状の導電体は、設地電位として用いてもよいが、プラズマ状態に対応して、電位を与えることによりさらに効果が上がる。また、第１の実施の形態では、チタン膜を１０９を堆積した例を示しているが、コバルト、ニッケル等の他の高融点金属を堆積するようにしても同様の効果が得られることは勿論である。

【００４５】次に図１（ｃ）に示すように、窒化雰囲気中で７００℃以下の急速熱処理（ＲＴＡ）することにより、多結晶シリコンであるゲート電極１０５の表面およびソース・ドレイン領域１０７および１０８と接触するチタン膜１０９の界面のみにＣ４９型構造のチタンシリサイド層１１０を形成する。また、この際、フィールド酸化膜１０３およびサイドウォール１０６と接触するチタン膜１０９と半導体基板上のチタン膜１０９の一部は窒化されて窒化チタン膜１１１となる。

【００４６】次に図１（ｄ）に示すように、アンモニア水および過酸化水素水等の混合液などにより、選択的にウェットエッチングし、未反応チタンと窒化チタン膜１１１のみを除去する。次いで、前述のＲＴＡよりも高温（８００℃以上）のＲＴＡを行い、前記のＣ４９型構造のチタンシリサイド層１１０よりも電気抵抗率の低いＣ５４型構造のチタンシリサイド１１２を形成する。

【００４７】このようにして製造されたＭＯＳ型電界効果トランジスタは、スパッタによるゲート耐圧の劣化が起こっておらず、良好なゲート耐圧が得られている。コリメート板６６がウェハー６３とターゲット６５間に挿入されているために、ウェハー６３に到達するはずの電荷がコリメート板６６に流れて、ゲート電極１０５のチャージアップが抑制されいるためである。

【００４８】このようにサリサイド構造を有したフローティングゲート電極上に高融点金属をスパッタ堆積する場合には、ウェハーへ到達する電荷量を制御する方法として、発生した電荷をウェハーに到達しないようにすることでゲート耐圧特性を向上させることができる。

本発明に係る半導体装置の製造方法の第２の実施形態

図２（ａ）に示すようにＰ型シリコン基板２０１にＮウェル２０２を既知の方法により形成する。次いで、Ｐ型シリコン基板２０１の表面にフィールド絶縁膜としてフィールド酸化膜２０３を選択酸化法により形成する。このフィールド酸化膜２０３に囲まれた活性領域に、順次シリコン酸化膜などのゲート絶縁膜２０４と多結晶シリコンを成長し、多結晶シリコンにリンを既知の手法によりドープして多結晶シリコンの電気抵抗の低減を図る。次いで、既知の手法であるフォトリソグラフィー法とドライエッチング法により、多結晶シリコンをパターンニングし図２（ａ）に示すように、ゲート電極２０５を形成する。

【００４９】次に、フォトリソグラフィー法とイオン注入法により、低濃度のＮ型不純物拡散層２１３と低濃度のＰ型不純物拡散層２１４を形成する。次いで、ゲート電極２０５の側面にシリコン酸化膜あるいはシリコン窒化膜から構成されるサイドウォール２０６を既知のＣＶＤ技術とエッチング技術を用いて形成する。

【００５０】次に、図２（ｂ）に示すようにフォトリソ

グラフィー法とイオン注入法により、Ｎ型不純物拡散層のソース・ドレイン領域２０７とＰ型不純物拡散層のソース・ドレイン領域２０８を形成する。次いで、ゲート電極２０５である多結晶シリコンの表面と半導体基板表面の自然酸化膜を除去し、例えばゲート電極に到達する電荷量Ｑが５Ｃ／ｃｍ^2 以下になるような条件とするマグネトロンスパッタ装置を用いて、高融点金属であるチタンをスパッタ堆積してチタン膜２０９を形成する。

【００５１】このときに使用するマグネトロンスパッタ装置の構成を図７（ｂ）、（ｄ）または（ｅ）に示す。従来のスパッタ装置として、図７（ａ）に示す如く、チャンバ７１内にウェハーホルダ７２上にウェハー７３が載置され、ウェハー７３に離間対向する位置にターゲット７４が配置された、ホルダーマグネットがない構造のスパッタ装置が知られているが、このものは発明者らの詳細な実験結果により、プラズマ７５のプラズマ密度が最大の領域が最もゲート初期耐圧劣化が見られた。

【００５２】これに対して、図７（ｂ）に示すマグネトロンスパッタ装置は、ホルダーマグネットがない構造のマグネトロンスパッタ装置において、プラズマ７７のプラズマ密度最大の領域が基板（ウェハー）外側になるように、大きさを設定したターゲット７６を用いた構造のマグネトロンスパッタ装置であり、上記のチタン膜２０９をスパッタ堆積した場合には、プラズマ７７から発生した電荷がウェハー７３に到達しないようにできるため、良好な電気特性が得られた。

【００５３】また、図７（ａ）及び（ｂ）に示したマグネトロンスパッタ装置は、プラズマ７５、７７がウェハー７３に直接接触している構造であるが、従来のマグネトロンスパッタ装置には図７（ｃ）に示すように、プラズマ８０がウェハー７３に接しない状態でホルダマグネット７９が装着されている構造のマグネトロンスパッタ装置も知られている。すなわち、この従来のマグネトロンスパッタ装置では、チャンバ７１内にウェハーホルダ７２上にホルダマグネット７９を介してウェハー７３が載置されており、ターゲット７４からのプラズマ８０はウェハー７３には接しない。

【００５４】しかし、この従来のマグネトロンスパッタ装置でも、プラズマから発生した電荷（Ar^+あるいは電子）がウェハー７３に到達することにより、同様にゲート初期耐圧不良が生じ、発明者の詳細な実験結果より、ウェハー７３周辺部にゲート初期耐圧の劣化箇所が見られた。

【００５５】そこで、このホルダーマグネットがある構造のマグネトロンスパッタ装置として、この実施の形態では、図７（ｄ）または図７（ｅ）に示した構造のマグネトロンスパッタ装置を使用してチタン膜２０９をゲート電極に到達する電荷量Ｑが５Ｃ／ｃｍ^2 以下になるような条件でスパッタ堆積する。図７（ｄ）に示すマグネトロンスパッタ装置は、プラズマを安定化させるために取り付けられているホルダマグネット８１を、ウェハー７３の側面を覆う形状とした点に特徴があり、これにより、プラズマ８２から発生した電荷を、ホルダマグネット８１の磁場によりトラップすることにより、ゲート初期耐圧不良を抑制することができる。

【００５６】また、図７（ｅ）に示すマグネトロンスパッタ装置は、プラズマを安定化させるために取り付けられているホルダマグネット８３の磁界強度を、プラズマ８４のプラズマ最大領域がウェハー８３より上部にあるように設定した点に特徴があり、これにより、プラズマ８４から発生した電荷を、ホルダマグネット８３の磁場によりトラップすることにより、ゲート初期耐圧不良を抑制することができる。

【００５７】図７（ｄ）あるいは図７（ｅ）に示した構造のマグネトロンスパッタ装置の場合には、ホルダマグネット８１、８３から発生した磁場により電荷がトラップされたことで、周辺部にも劣化箇所は見られず良好な電気特性が得られた。実際には、マグネトロンスパッタ装置の構造によってゲート初期耐圧の劣化の程度が変化するため、上述のプラズマ最大領域を変更する方法とウェハー側のホルダマグネットにより発生する磁場によってトラップする方法の組み合わせで最適化する場合も考えられる。

【００５８】この第２の実施の形態では、チタンを堆積した例を示しているが、コバルト、ニッケル等の他の高融点金属を堆積するようにしても同様の効果が得られることは勿論である。

【００５９】再び図２に戻って説明するに、次に図２（ｃ）に示すように窒素雰囲気中で７００℃以下の急速熱処理（ＲＴＡ）をすることにより、多結晶シリコンであるゲート電極２０５の表面およびソース・ドレイン領域１０７および１０８と接触するチタン膜１０９の界面のみにＣ４９型構造のチタンシリサイド２１０を形成する。また、この際、図２（ｃ）に示すように、フィールド酸化膜２０３およびサイドウォール２０６と接触するチタン膜２０９と半導体基板上のチタン膜２０９の一部は窒化されて窒化チタン膜２１１となる。

【００６０】次に、図２（ｄ）に示すように、アンモニア水および過酸化水素水等の混合液などにより、選択的にウェットエッチングし、未反応チタンと窒化チタン膜２１１のみを除去する。次いで、前述のＲＴＡよりも高温（８００℃以上）のＲＴＡを行い、前記のＣ４９型構造のチタンシリサイド２１０よりも電気抵抗率の低いＣ５４型構造のチタンシリサイド２１２を形成する。

【００６１】この実施の形態では、マグネトロンスパッタ装置構成を図７（ｂ），（ｄ）または（ｅ）のような構造にすることで、プラズマから発生する電荷がウェハーに到達せず、ゲート初期耐圧劣化が抑えられる。更に、第１の実施の形態で用いるマグネトロンスパッタ装置では導電体の網状のコリメート板を挿入しているた

め、スパッタされた膜が導電体の網状のコリメート板に堆積されることによりウェハー上へのスパッタレートの低下やパーティクル等の問題のため、コリメート板の交換の必要があるのに対し、この第２の実施の形態で用いるマグネトロンスパッタ装置では、導電体の網状のコリメート板を挿入していないため、コリメート板の交換の必要がなくなり、装置を安定に維持し易いという利点もある。

【００６２】なお、以上の第１および第２の実施の形態では、ゲート及び拡散層上に同時にシリサイドを形成する方法について示したが、ポリサイドゲート（WSix/Poly-Si）、ポリタメルゲート（W/WNx/Poly-Si）あるいは、メタルゲート（W/SiO_2）構造等のフローティングゲート上に高融点金属をスパッタして拡散層上にシリサイドを形成する場合についても、本発明を適用できることは勿論である。

【００６３】本発明に係るスパッタ装置の実施形態例
本実施形態例は、本発明に係るスパッタ装置をマグネトロンスパッタ装置に適用した実施形態の一例であって、図１０（ａ）は本実施形態例のマグネトロンスパッタ装置の構成を示す模式的断面図、図１０（ｂ）はコリメート板の平面図、図１０（ｃ）はコリメート板の側面図である。図１０中、図８と同じ部品、部位には同じ符号を付している。本実施形態例のマグネトロンスパッタ装置３０は、図１０に示すように、基本的には、前述の図６に示したマグネトロンスパッタ装置と同じ構成を備えており、スパッタ・チャンバ１２内に、ウェハーWを載置させるウェハーホルダ１４と、ウェハーWに対して離間、対面する位置にターゲットTを保持するカソードマグネット１６と、ウェハーホルダ１４とカソードマグネット１６との間に設けられた網板状のコリメート板３２とを備えている。

【００６４】コリメート板３２は、スパッタ粒子の異方性を高めると共に荷電粒子を捕捉するために設けられており、図１０（ｂ）に示すように、正六角形を連続させた網形状の、導電体からなる網状板として構成され、接地されている。コリメート板３２の正六角形の網目又は孔は、ターゲットTからウェハーWに向かって貫通し、網目又は孔のアスペクト比は１である。即ち、コリメート板の厚さｔ（図１０（ｃ）参照）と網目又は孔の径D（網目又は孔の最大径、図１０（ｂ）参照）とは同じ長さである。また、コリメート板３２は、位置調整機構３４により、コリメート板３２の面からカソードマグネット１６のターゲット保持面までの距離（Ｔ／Ｃ間距離、図１０（ａ）では、L_1 で表示）が変更され、その位置に保持されるようになっている。位置調整機構３４は、既知の機構であって、油圧シリンダ、エアシリンダ等の駆動装置によりコリメート板３２を上下に自在に昇降させる。なお、コリメート板３２の広さは、コリメート板３２がウェハーWの全面を覆っている必要もなく、プラズマ強度分布が高い、あるいは荷電粒子が発生しやすい領域だけをカバーしておればよい。

【００６５】実験例１
アネルバ（株）製のモデル番号Ｉ－１０６０にコリメート板を装着した、本実施形態例のマグネトロンスパッタ装置３０と同じ構成の実験装置を使って、スパッタリング実験を行った。以下に、実験装置の仕様を簡単に示す。

ターゲット
厚さ　　：３㎜
直径　　：１２インチ
ウェハーホルダ
ウェハー寸法：６インチ径又は８インチ径
チャック方式：クランプチャック
コリメート板
孔径D　　：２３㎜
厚さｔ　　：２３㎜
孔の形状　：正六角形の連続形状
アスペクト比：１
材質　　：ステンレス鋼

【００６６】上述の実験装置で、カソードマグネット１６のターゲット保持面とウェハーWの表面との距離（Ｔ／Ｓ間距離、図１０（ａ）では、L_2 で表示）を１０３㎜に調整し、かつカソードマグネット１６のターゲット保持面とコリメート板３２の対向面との距離L_1 を３４㎜にに調整して、ウェハーホルダ１４とカソードマグネット１６との間に印加するスパッタ電力を１．０ｋW、１．５ｋW及び２．０ｋWに変えて、以下のスパッタリング条件でＣｏをスパッタし、膜厚１００ÅのＣｏ膜を図９に示すポリシリコン膜上に成膜した。

スパッタリング条件
ホルダ温度　：室温
チャンバ圧力：３～８mTorr

次いで、ゲート酸化膜の絶縁耐圧の良否をチップ毎に調べ、図１２（ａ）～（ｃ）に示すように、ゲート酸化膜の重度絶縁不良のチップを黒色、及び軽度絶縁不良のチップを灰色に彩色した。

【００６７】実験例２
実験例１と同じ実験装置を使い、カソードマグネット１６のターゲット保持面とウェハーWの表面との距離L_2を１１３㎜に調整し、かつカソードマグネット１６のターゲット保持面とコリメート板３２の対向面との距離L_1を２４㎜、２９㎜、３４㎜、３９㎜、４４㎜及び５６㎜に変更し、かつ同じL_1でウェハーホルダ１４とカソードマグネット１６との間に印加するスパッタ電力を１．０ｋW、１．５ｋW及び２．０ｋWに変えて、計１８回の相互に異なる条件でＣｏスパッタリングを行った。尚、その他の条件は、実験例１と同じスパッタリング条件と同じである。次いで、ゲート酸化膜の絶縁耐圧の良否をチップ毎に調べ、図１３（ａ）～（ｃ）から図

１８（ａ）～（ｃ）に示すように、ゲート酸化膜の重度絶縁不良のチップを黒色、及び軽度絶縁不良のチップを灰色に彩色した。

【００６８】図１９に示すように、スパッタ電力をパラメータとして、実験例１と２の実験結果を集計した。図１９では、横軸にL_1、縦軸にゲート酸化膜の良品率（％）を取っている。図１９から判る通り、スパッタ電力の大小にかかわらず、L_1が３９㎜以下では、良品率がほぼ１００％に達し、一方、L_1が４４㎜以上では、良品率は６０％以下に急激に低下する。即ち、ゲート酸化膜の良品率、即ちコリメート板３２の介在効果に関し、コリメート板３２のターゲット、又はカソードマグネットに対する明確な臨界的位置が、３９㎜と４４㎜の間に存在することが判る。図１９の左端の棒グラフは、コリメート板を介在させないときの良品率の数値であって、L_1が５６㎜のときの良品率とほぼ同じである。

【００６９】実験例３

実験例１と同じ実験装置を使い、カソードマグネットに対するコリメート板の距離L_1を２９㎜、カソードマグネットとウェハーホルダとの距離L_2を６８㎜に設定して、以下のスパッタリング条件の下でスパッタ電力（ｋＷ）とゲート酸化膜の良品率との関係を調べ、その結果を図２０に示した。また、比較のために、コリメート板を備えていないこと除いて実験装置と同じ構成のマグネトロンスパッタ装置を使って、スパッタリングを行い、その結果も合わせて図２０に示した。

スパッタリング条件

チャンバ圧力　：８～１０mTorr

ガス流量　　：８０～１００scc/m

スパッタパワー：１．５ｋＷ

図２０から判る通り、本発明で特定した距離関係でコリメート板を設けることにより、コリメート板を備えないマグネトロンスパッタ装置に比べて、本実施形態例のマグネトロンスパッタ装置は、ゲート酸化膜の良品率のスパッタ電力依存性が極めて低い。

【００７０】実験例４

実験例１と同じ実験装置を使い、カソードマグネットに対するコリメート板の距離L_1を２９㎜、カソードマグネットとウェハーホルダとの距離L_2を６８㎜に設定して、以下のスパッタリング条件の下でスパッタレート（Å／sec ）とゲート酸化膜の良品率の関係を調べ、その結果を図２１に表示した。また、比較のために、コリメート板を備えていないこと除いて本実施形態例の同じ構成のマグネトロンスパッタ装置を使って、スパッタリングを行い、その結果も合わせて図２１に表示した。

スパッタリング条件

チャンバ圧力　：８～１０mTorr

ガス流量　　：８０～１００scc/m

スパッタパワー：１．５ｋＷ

図２１から判る通り、本発明で特定した距離関係でコリメート板を設けることにより、コリメート板を備えないマグネトロンスパッタ装置に比べて、本実施形態例のマグネトロンスパッタ装置は、良品率のスパッタレート依存性が低い。

【００７１】ところで、スパッタレートを上げることにより、導電性の金属（もしくは金属珪化物）がウェハー表面を速やかに覆うため、荷電粒子はゲートの深さ方向よりもウェハの水平方向に進むようになり、ゲート酸化膜の初期耐圧劣化確率は低くなる。従って、スパッタレートを上げることは、図２１に示すように、ゲート酸化膜の初期絶縁耐圧の劣化防止に有効である。但し、スパッタレートが速過ぎると、ウェハーの面内膜厚分布差が増大し、更には高温スパッタ時のシリサイド化反応量の減少なども懸念されるために、高スパッタレートでのスパッタは、余り好ましくない。実験例３のスパッタパワーを２．６ｋＷにすることで、スパッタレートを上げると、コリメート板をカソードマグネット１６のカソード保持面に対する距離を５０㎜にした場合でも、良品率は９８％であることが検証された。なお、スパッタレートを上げてゲート酸化膜の絶縁耐圧の劣化防止を図ろうとしても、スパッタが始まった直後には荷電粒子のゲートへの飛来を遮断する導電性の金属膜が成膜されていないので、コリメート板を介在させた場合に比べて、ゲート酸化膜の初期耐圧劣化防止の効果が低い。また、装置メーカの異なるエンジュラ（AMAT ENDURA ）での結果で、４６．５㎜でも満足する結果が得られた。

【００７２】実験例５

実験例１及び実験例２で使用した本実施形態例のマグネトロンスパッタ装置を使い、カソードマグネットに対するコリメート板の距離L_1を３４㎜、カソードマグネットとウェハーホルダとの距離L_2を１０３㎜に設定し、印加電圧を１．５ｋＷに固定し、かつガス圧を５mTorr、８㎜Torr、１０mTorr、及び１５mTorrに設定して、それぞれ、Ｃｏスパッタリングを行い、ゲート酸化膜の良品率のガス圧依存性を関係を調べた。その結果、５mTorr、８㎜Torr、１０mTorr、及び１５mTorrのガス圧で、ゲート酸化膜の良品率は、それぞれ、１００％であって、コリメート板を設けたマグネトロンスパッタ装置では、ゲート酸化膜の良品率には、ガス圧依存性が無いことが判った。

【００７３】以上の実験例１から実験例５の結果から、本実施形態例のスパッタ装置は、カソードマグネット１６のカソード保持面に対して距離２４㎜以上５０㎜以下の範囲にコリメート板３２を配置させることにより、ゲート電極に高融点金属シリサイド膜を形成する際、ゲート酸化膜の絶縁耐圧の劣化が生じないようにして、高融点金属をポリシリコン膜上にスパッタできるスパッタ装置であることが実証されている。また、本実施形態例のスパッタ装置は、ゲート酸化膜の良品率に関し、スパッタ電力依存性、スパッタレート依存性及びガス圧依存性

が低く、スパッタリング条件を広い範囲で設定することができる。

【００７４】

【発明の効果】以上説明したように、本発明によれば、半導体基板上に選択的に形成される絶縁膜間に高融点金属シリサイド層を形成する半導体装置の製造方法において、ゲート耐圧の劣化が生じない条件で高融点金属をスパッタ堆積するようにしたため、高融点金属シリサイド層を形成することにより低抵抗化を図るＭＯＳ型電界効果トランジスタ（ＭＯＳＦＥＴ）を、ゲート絶縁膜の薄膜化や高集積化により微細化した場合でも、より信頼性高く製造することができる。

【００７５】本発明に係るスパッタ装置によれば、ターゲットホルダと、ウェハーホルダとの間に、ターゲットからウェハーに向けて貫通した多数の貫通孔を有する導電体からなるコリメート板を接地した状態で介在させることにより、好適には、コリメート板をターゲットホルダーに対して第１の間隔D_1 以下で第２の間隔D_2 以上の範囲の間隔で配置することにより、ゲート電極に高融点金属シリサイド膜を形成する際、ゲート酸化膜の絶縁耐圧の劣化が生じないようにして、高融点金属をポリシリコン膜上にスパッタできるスパッタ装置を実現している。また、本発明に係るスパッタ装置は、ゲート酸化膜の良品率に関し、スパッタ電力依存性、スパッタレート依存性及びガス圧依存性が低く、スパッタリング条件を広い範囲で設定することができる。

【図面の簡単な説明】

【図１】本発明の第１の実施の形態の各工程での素子断面図である。

【図２】本発明の第２の実施の形態の各工程での素子断面図である。

【図３】従来方法の一例の各工程での素子断面図。

【図４】従来のスパッタ条件で行った場合のゲート耐圧の良品率等を示す図である。

【図５】コリメート板を挿入した場合のゲート耐圧特性の良品率等を示す図である。

【図６】本発明の第１の実施の形態で使用するスパッタ装置の構成図である。

【図７】本発明の第２の実施の形態で使用する各例のスパッタ装置と従来のスパッタ装置の構成図である。

【図８】従来のスパッタ装置の構成を示す模式図である。

【図９】シリサイド化の説明図である。

【図１０】図１０（ａ）は実施形態例のスパッタ装置の構成を示す模式図、図１０（ｂ）はコリメート板の平面図、図１０（ｃ）はコリメート板の側面図である。

【図１１】従来のスパッタ装置を使ってスパッタリングした際のゲート酸化膜劣化を示すウェハーマップである。

【図１２】図１２（ａ）～（ｃ）は、それぞれ、本実施形態例のスパッタ装置を使って、相互に異なる条件下でスパッタした際のゲート酸化膜劣化を示すウェハーマップである。

【図１３】図１３（ａ）～（ｃ）は、それぞれ、本実施形態例のスパッタ装置を使って、相互に異なる条件下でスパッタした際のゲート酸化膜劣化を示すウェハーマップである。

【図１４】図１４（ａ）～（ｃ）は、それぞれ、本実施形態例のスパッタ装置を使って、相互に異なる条件下でスパッタした際のゲート酸化膜劣化を示すウェハーマップである。

【図１５】図１５（ａ）～（ｃ）は、それぞれ、本実施形態例のスパッタ装置を使って、相互に異なる条件下でスパッタした際のゲート酸化膜劣化を示すウェハーマップである。

【図１６】図１６（ａ）～（ｃ）は、それぞれ、本実施形態例のスパッタ装置を使って、相互に異なる条件下でスパッタした際のゲート酸化膜劣化を示すウェハーマップである。

【図１７】図１７（ａ）～（ｃ）は、それぞれ、本実施形態例のスパッタ装置を使って、相互に異なる条件下でスパッタした際のゲート酸化膜劣化を示すウェハーマップである。

【図１８】図１７（ａ）～（ｃ）は、それぞれ、本実施形態例のスパッタ装置を使って、相互に異なる条件下でスパッタした際のゲート酸化膜劣化を示すウェハーマップである。

【図１９】スパッタ電力をパラメータとして、実験例１と２の実験結果を集計したグラフである。

【図２０】良品率のスパッタパワー依存性を示すグラフである。

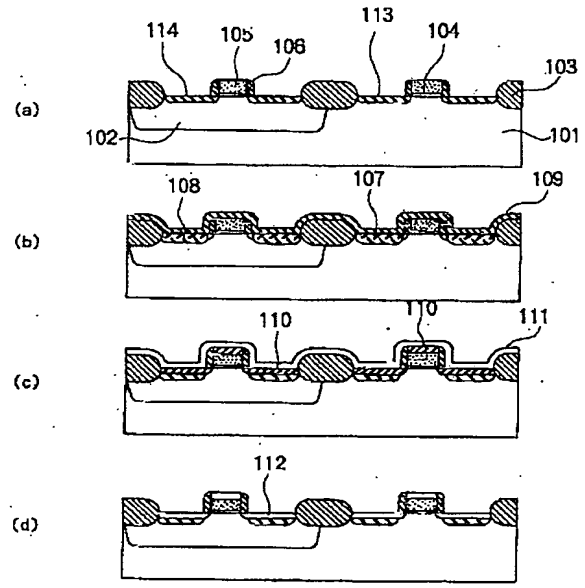
【図２１】良品率のスパッタレート依存性を示すグラフである。

【符号の説明】

１０　従来のスパッタ装置
１２　スパッタ・チャンバ
１４　ウェハーホルダ
１６　カソードマグネット
２０　シリコン基板
２２　ポリシリコン膜
２４　Ｃｏ膜
２６　サイドウォール
２８　ゲート酸化膜
３０　実施形態例のスパッタ装置
３２　コリメート板
３４　位置調整機構
６１、７１　チャンバ
６２、７２　ウェハーホルダ
６３、７３　ウェハー
６５、７４、７６　ターゲット

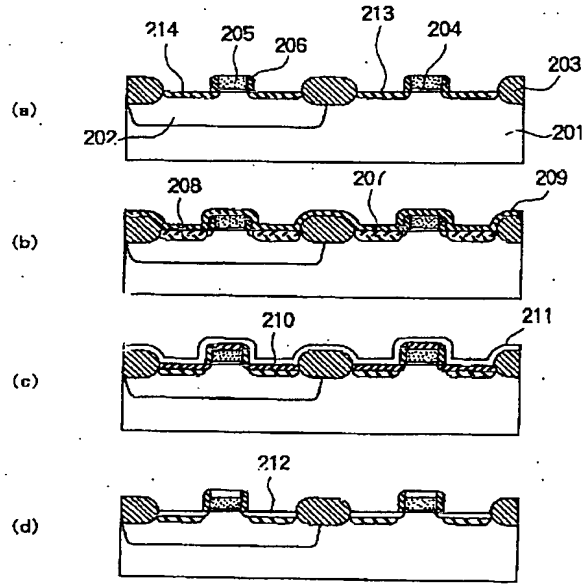
６６　コリメート板
７５、７７、８０、８２、８４　プラズマ
７９、８１、８３　ホルダマグネット
１０１、２０１　Ｐ型シリコン基板
１０２、２０２　Ｎウェル
１０３、２０３　フィールド酸化膜
１０４、２０４　ゲート絶縁膜
１０５、２０５　ゲート電極
１０６、２０６　サイドウォール
１０７、２０７　Ｎ型ソース・ドレイン領域
１０８、２０８　Ｐ型ソース・ドレイン領域
１０９、２０９　チタン膜
１１０、２１０　Ｃ４９型構造のチタンシリサイド層
１１１、２１１　窒化チタン膜
１１２、２１２　Ｃ５４型構造のチタンシリサイド層
１１３、２１３　Ｎ型不純物拡散層
１１４、２１４　Ｐ型不純物拡散層

【図１】



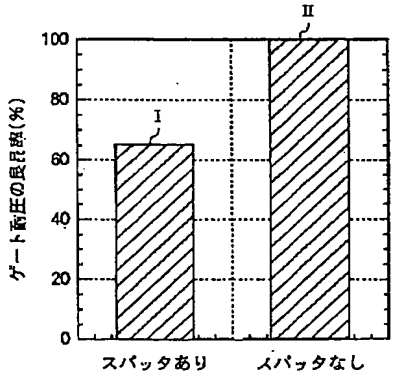
101 ：Ｐ型シリコン基板　107 ：Ｎ型ソース・ドレイン領域
102 ：Ｎ型ウェル　108 ：Ｐ型ソース・ドレイン領域
103 ：フィールド酸化膜　109 ：チタン膜
104 ：ゲート絶縁膜　110 ：C49型構造のチタンシリサイド層
105 ：ゲート電極　111 ：窒化チタン膜
106 ：サイドウォール　112 ：C54構造のチタンシリサイド層

【図２】

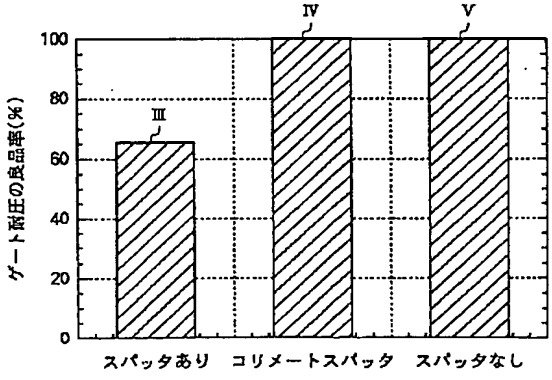


201 ：Ｐ型シリコン基板　207 ：Ｎ型ソース・ドレイン領域
202 ：Ｎ型ウェル　208 ：Ｐ型ソース・ドレイン領域
203 ：フィールド酸化膜　209 ：チタン膜
204 ：ゲート絶縁膜　210 ：C49型構造のチタンシリサイド層
205 ：ゲート電極　211 ：窒化チタン膜
206 ：サイドウォール　212 ：C54構造のチタンシリサイド層

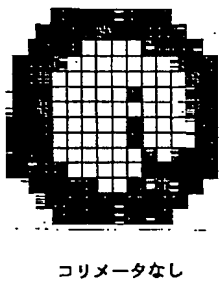
【図４】



【図５】

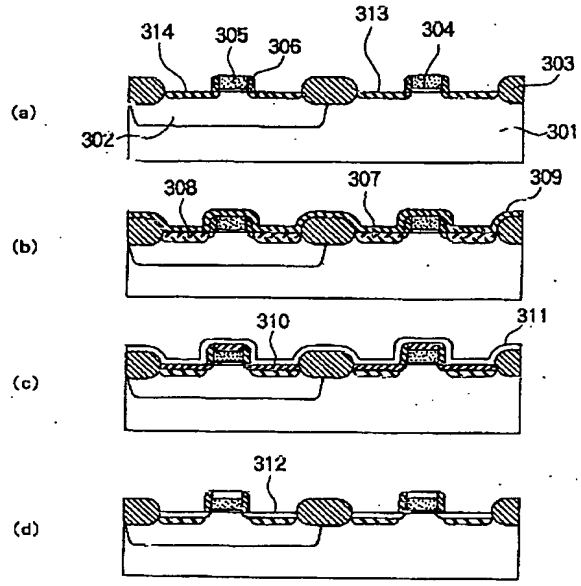


【図１１】



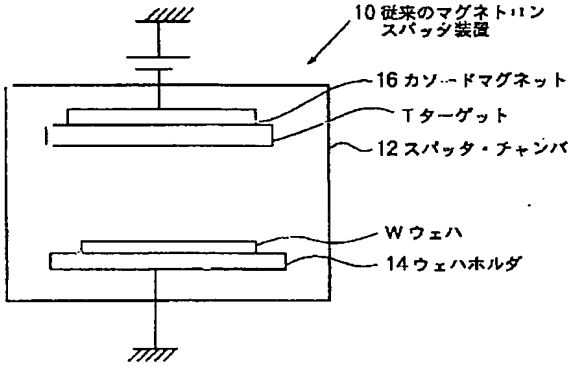
コリメータなし

【図3】



301：P型シリコン基板　307：N型ソース・ドレイン領域
302：N型ウェル　308：P型ソース・ドレイン領域
303：フィールド酸化膜　309：チタン膜
304：ゲート絶縁膜　310：C49型構造のチタンシリサイド層
305：ゲート電極　311：窒化チタン膜
306：サイドウォール　312：C54構造のチタンシリサイド層

【図8】



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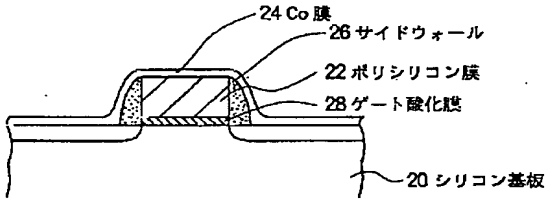

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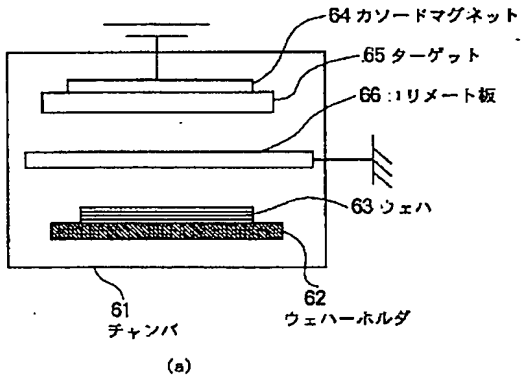
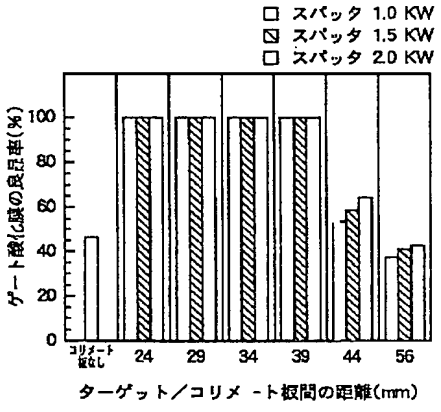
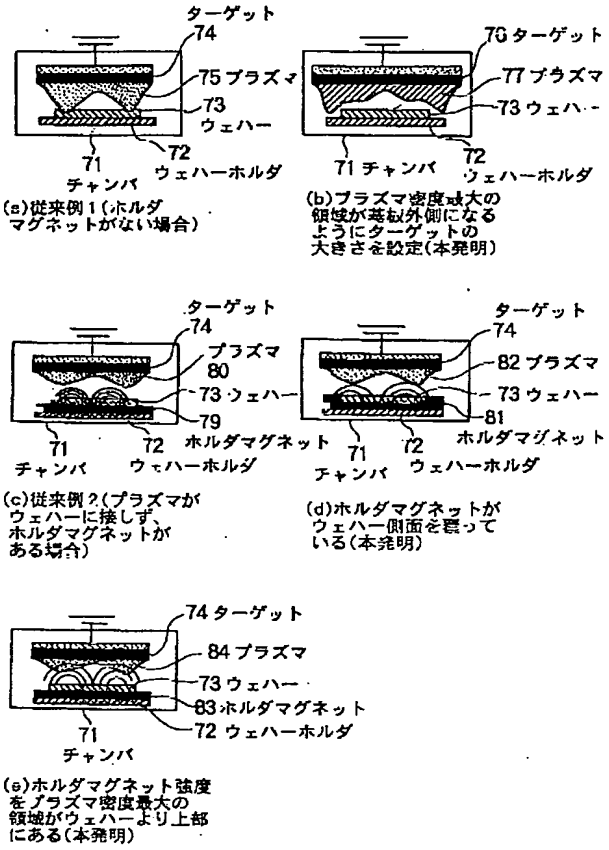


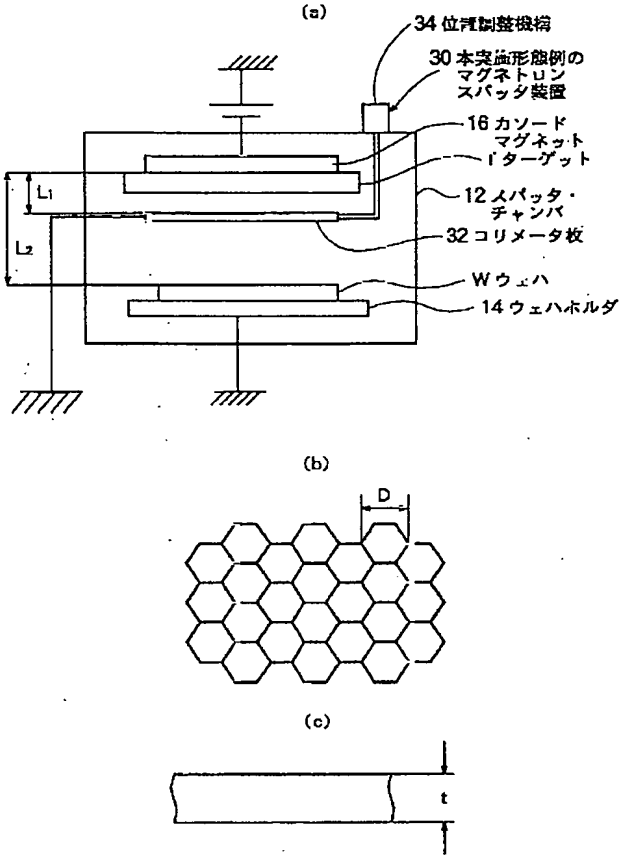
【図19】



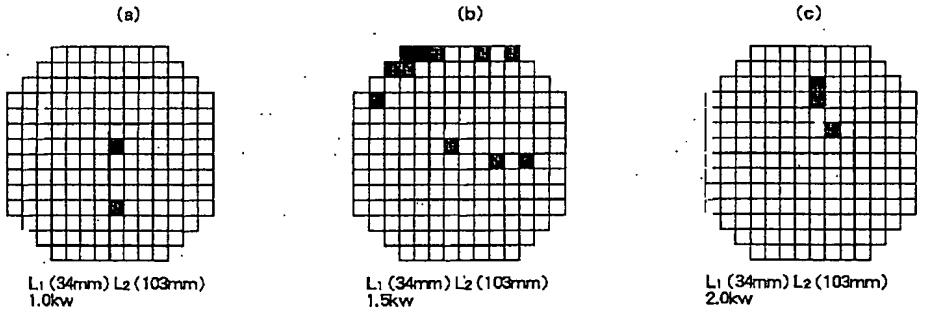
【図７】


ターゲット
74
75 プラズマ
73
ウェハー
71
チャンバ
72
ウェハーホルダ
(a)従来例１(ホルダ
マグネットがない場合)
76 ターゲット
77 プラズマ
73 ウェハー
71 チャンバ
72
ウェハーホルダ
(b)プラズマ密度最大の
領域が基板外側になる
ようにターゲットの
大きさを設定(本発明)
ターゲット
74
プラズマ
80
73 ウェハー
79
ホルダマグネット
71
チャンバ
72
ウェハーホルダ
(c)従来例２(プラズマが
ウェハーに接しず、
ホルダマグネットが
ある場合)
ターゲット
74
82 プラズマ
73 ウェハー
81
ホルダマグネット
71
チャンバ
72
ウェハーホルダ
(d)ホルダマグネットが
ウェハー側面を覆って
いる(本発明)
74 ターゲット
84 プラズマ
73 ウェハー
83 ホルダマグネット
72 ウェハーホルダ
71
チャンバ
(e)ホルダマグネット強度
をプラズマ密度最大の
領域がウェハーより上部
にある(本発明)

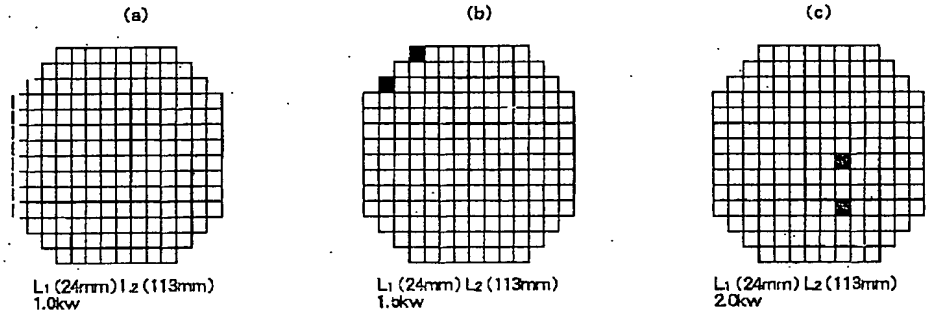
【図１０】


(a)
34 位置調整機構
30 本実施形態例の
マグネトロン
スパッタ装置
16 カソード
マグネット
ターゲット
12 スパッタ・
チャンバ
32 コリメータ板
L1
L2
W ウェハ
14 ウェハホルダ
(b)
D
(c)
t

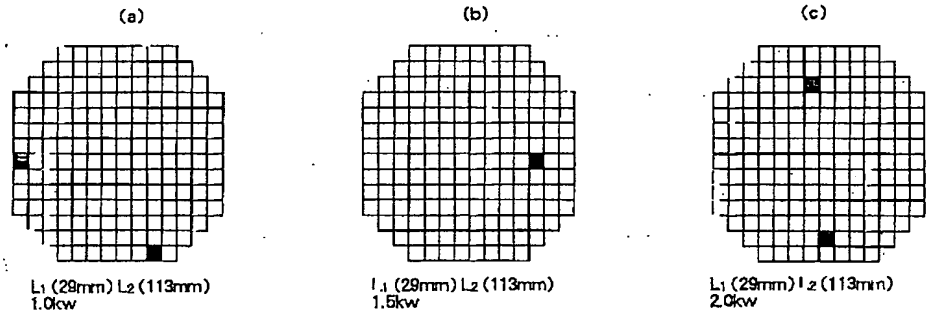
【図１２】


(a)
L1 (34mm) L2 (103mm)
1.0kw
(b)
L1 (34mm) L2 (103mm)
1.5kw
(c)
L1 (34mm) L2 (103mm)
2.0kw

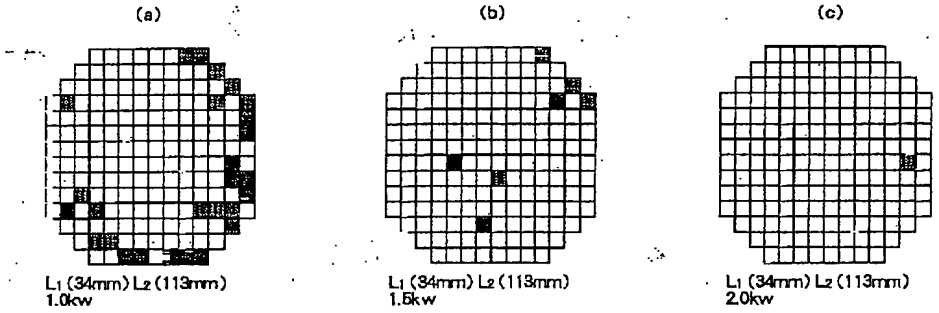
【図１３】



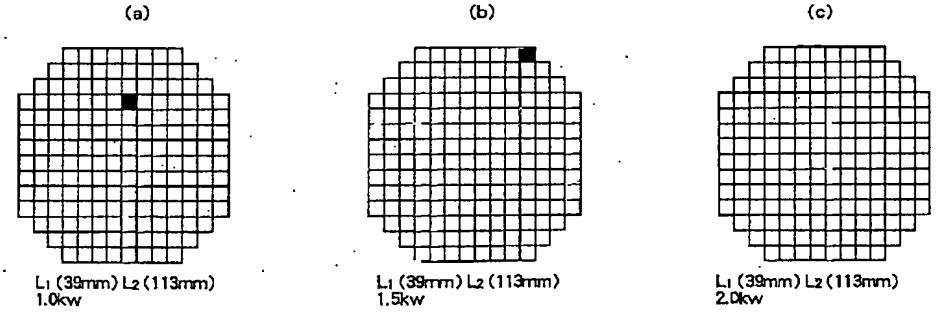
【図１４】



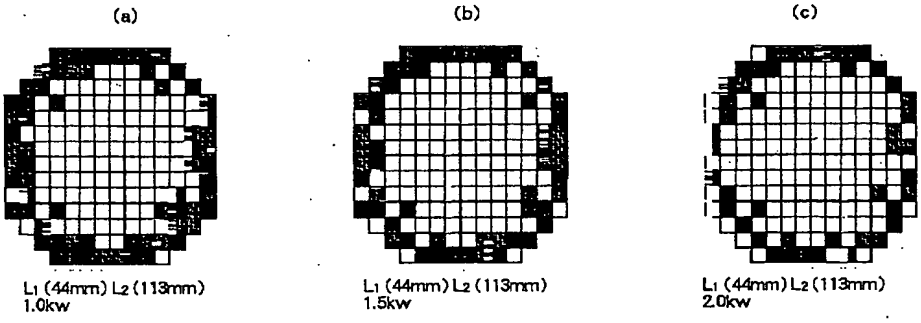
【図１５】



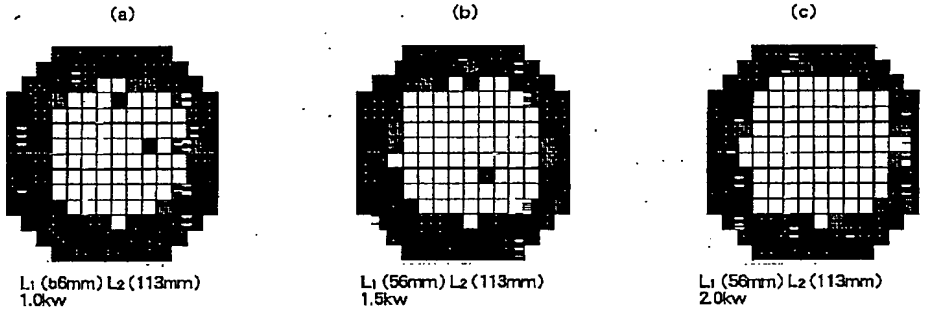
【図１６】



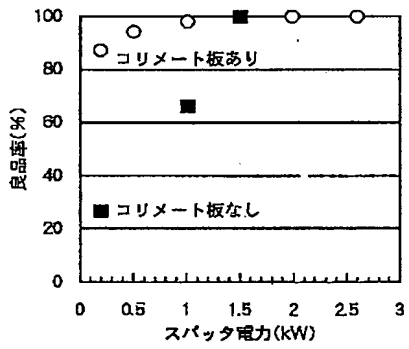
【図１７】



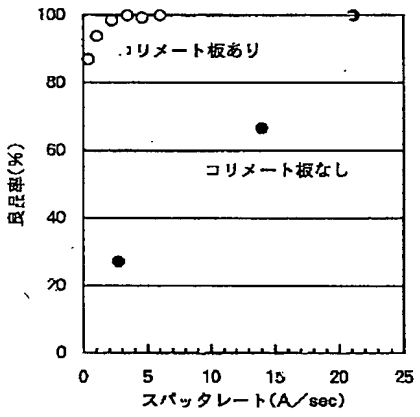
【図１８】



【図２０】



【図２１】



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